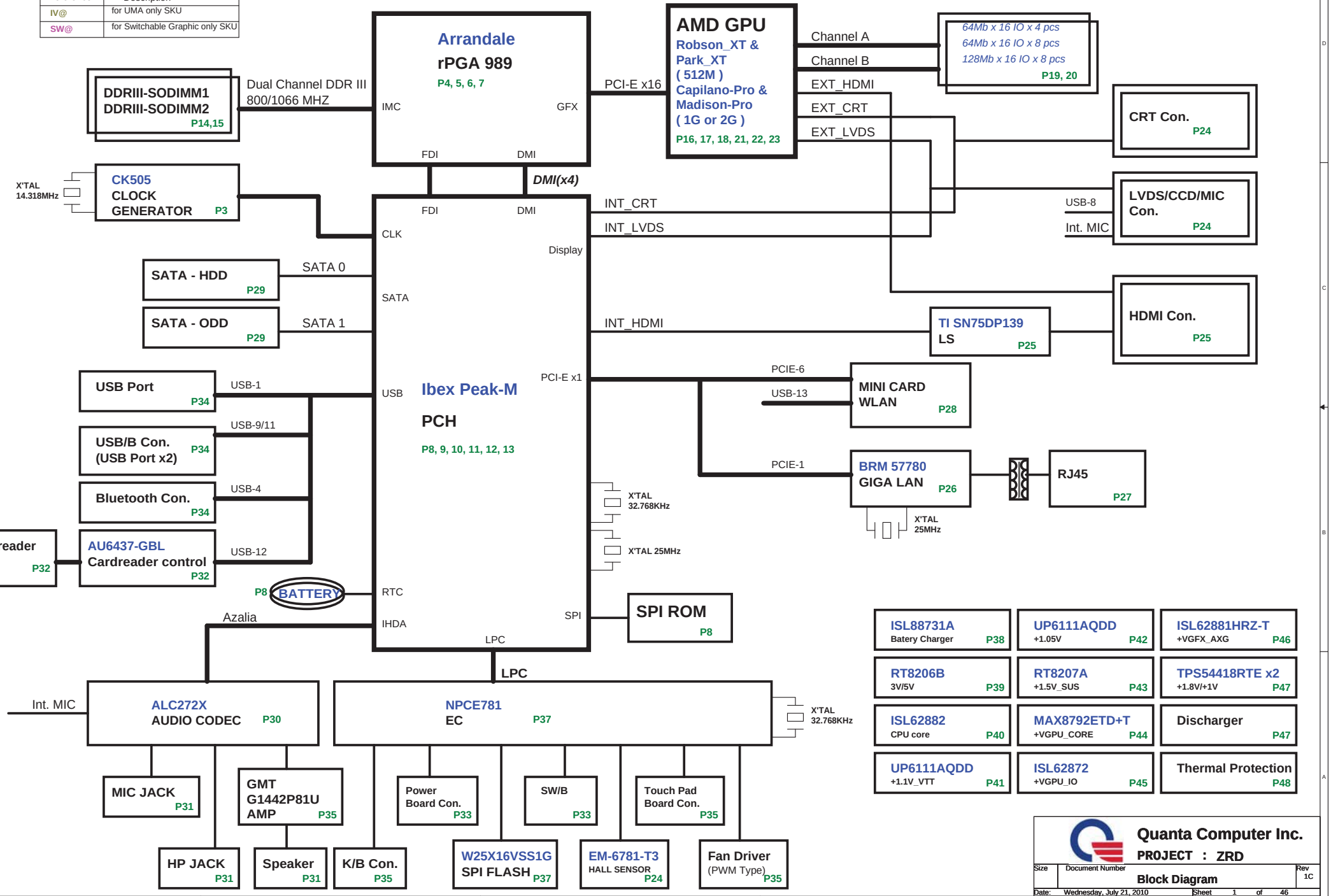
# HM55_CP (ZRD) SYSTEM BLOCK DIAGRAM

**BOM Option Table**

| Reference | Description |
|---|---|
| IV@ | for UMA only SKU |
| SW@ | for Switchable Graphic only SKU |

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|---|---|---|
| | Block Diagram | 1C |

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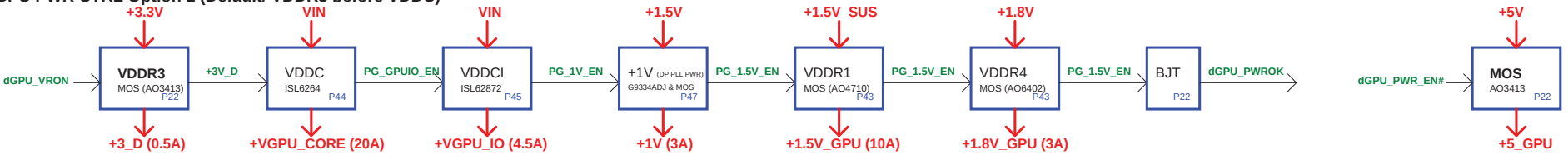
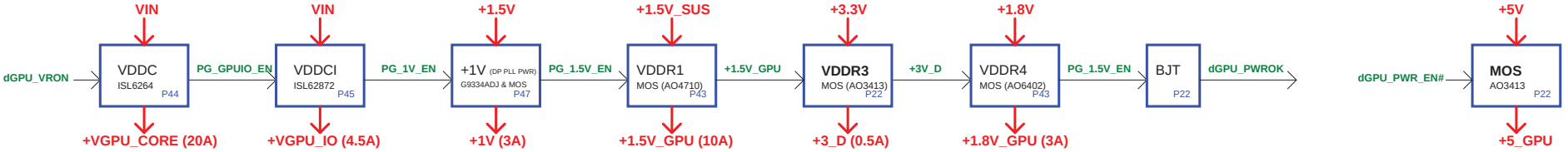
## GPU PWR CTRL Option 1 (Default/ VDDR3 before VDDC)



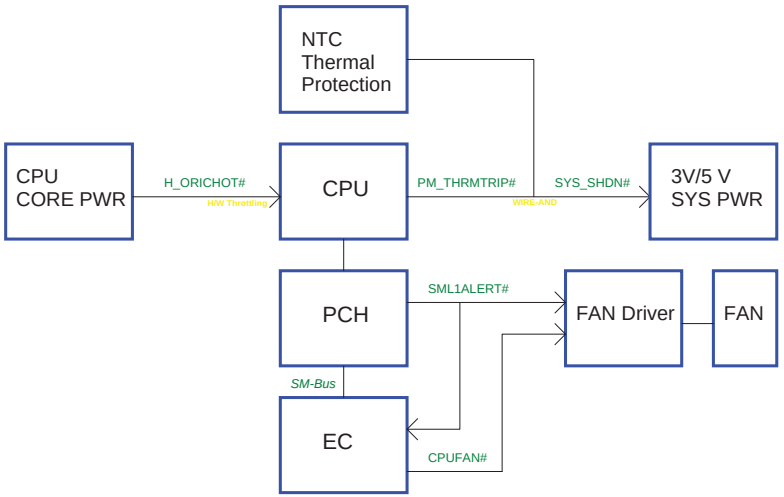

## GPU PWR CTRL Option 2 (VDDR3 after VDDR1)




## Power States

| POWER PLANE | VOLTAGE | DESCRIPTION | CONTROL SIGNAL | ACTIVE IN |
|---|---|---|---|---|
| VIN | +10V~+19V | MAIN POWER | ALWAYS | ALWAYS |
| +VCCRTC | +3V~+3.3V | RTC POWER | ALWAYS | ALWAYS |
| +3VPCU | +3.3V | EC POWER | ALWAYS | ALWAYS |
| +5VPCU | +5V | CHARGE POWER | ALWAYS | ALWAYS |
| +15V | +15V | CHARGE PUMP POWER | ALWAYS | ALWAYS |
| +3V_S5 | +3.3V | LAN/BT/CIR POWER | S5_ON | S0-S5 |
| +5V_S5 | +5V | USB POWER | S5_ON | S0-S5 |
| +5V | +5V | HDD/ODD/Codec/TP/CRT/HDMI POWER | MAINON | S0 |
| +3V | +3.3V | PCH/GPU/Peripheral component POWER | MAINON | S0 |
| +1.5VSUS | +1.5V | CPU/SODIMM CORE POWER | SUSON | S0-S3 |
| +0.75V_DDR_VTT | +0.75V | SODIMM Termination POWER | MAINON | S0 |
| +VGFX_AXG | variation | Internal GPU POWER | GFX_ON | S0 |
| +1.8V | +1.8V | CPU/PCH/Braidwood POWER | MAINON | S0 |
| +1.5V | +1.5V | MINI CARD/NEW CARD POWER | MAINON | S0 |
| +1.1V_VTT | +1.05V or +1.1V | CPU VTT POWER | MAINON | S0 |
| +1.05V | +1.05V | PCH CORE POWER | MAINON | S0 |
| +VCC_CORE | variation | CPU CORE POWER | VRON | S0 |
| LCDVCC | +3.3V | LCD POWER | LVDS_VDDEN | S0 |
| +5V_GPU | +5V | SWITCHABLE PWM IC POWER | dGPU_PWR_EN# | Discrete enable |
| +GPU_CORE | +0.9V~+1.1V | GPU CORE POWER | +3V_D | Discrete enable |
| +GPU_IO | +0.9V~+1.1V | GPU I/O POWER | PG_GPUIO_EN | Discrete enable |
| +1.5V_GPU | +1.5V | VRAM CORE POWER | PG_1.5V_EN | Discrete enable |
| +1.8V_GPU | +1.8V | GPU_CRE/LVDS/PLL POWER | +1.5V_GPU | Discrete enable |
| +1V | +1V | DP/PEG POWER | PG_1V_EN | Discrete enable |

## Thermal Follow Chart

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|---|---|---|
| | PWR Status & GPU PWR CRL & THRM | 1C |

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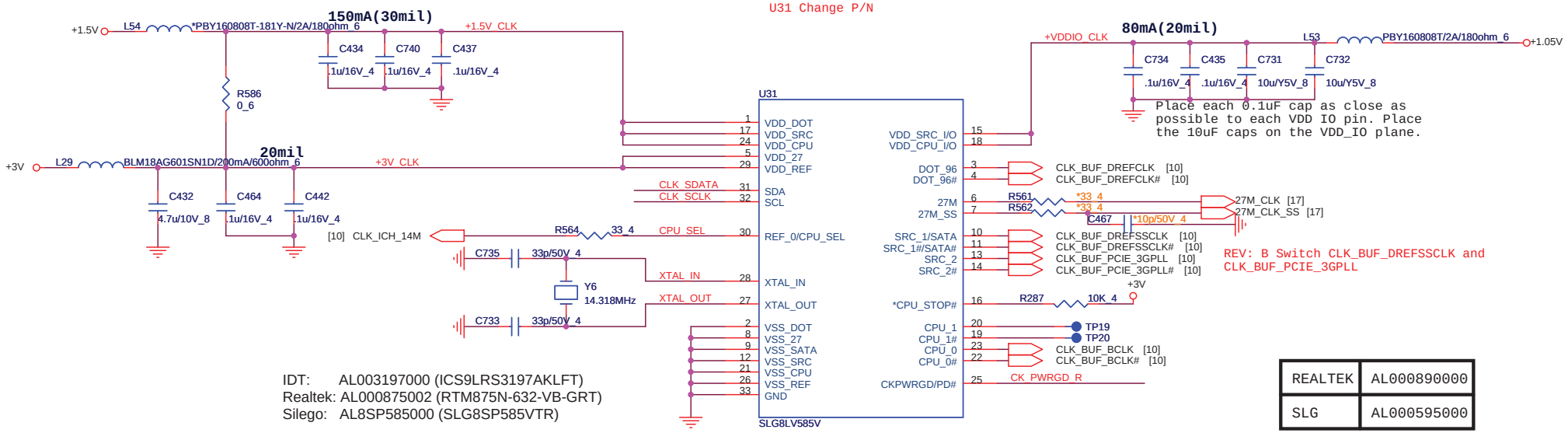
6/21 add R586 for 3V CLK gen
Un-stuff L54
U31 Change P/N

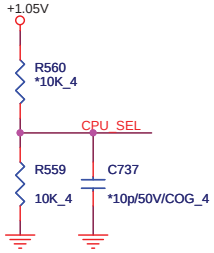



REV: B Switch CLK_BUF_DREFSSCLK and CLK_BUF_PCIE_3GPLL

IDT: AL003197000 (ICS9LRS3197AKLFT)
Realtek: AL000875002 (RTM875N-632-VB-GRT)
Silego: AL8SP585000 (SLG8SP585VTR)

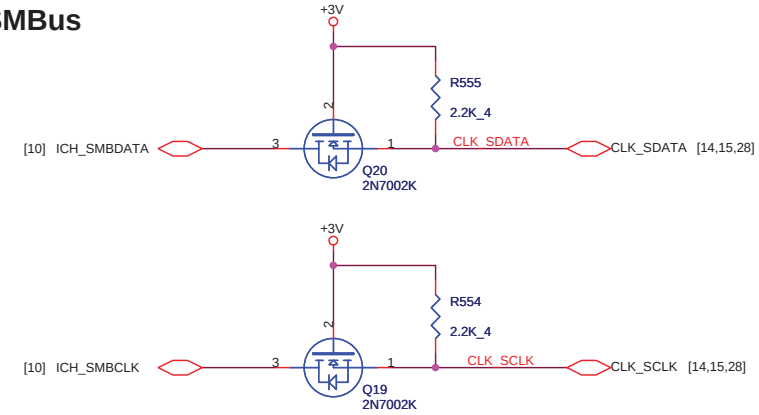
| | |
|---|---|
| REALTEK | AL000890000 |
| SLG | AL000595000 |

## CPU_CLK select

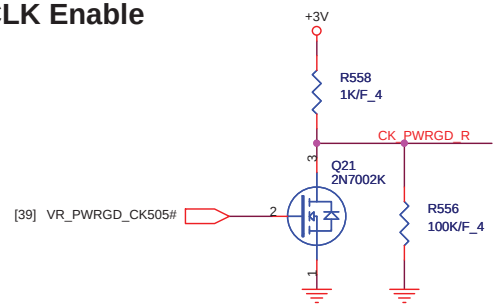



| | 0 | 1 |
|---|---|---|
| CPU_SEL | CPU0/1=133MHz (default) | CPU0/1=100MHz |

## SMBus




## CLK Enable

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|---|---|---|
| | Clock Generator | 1C |
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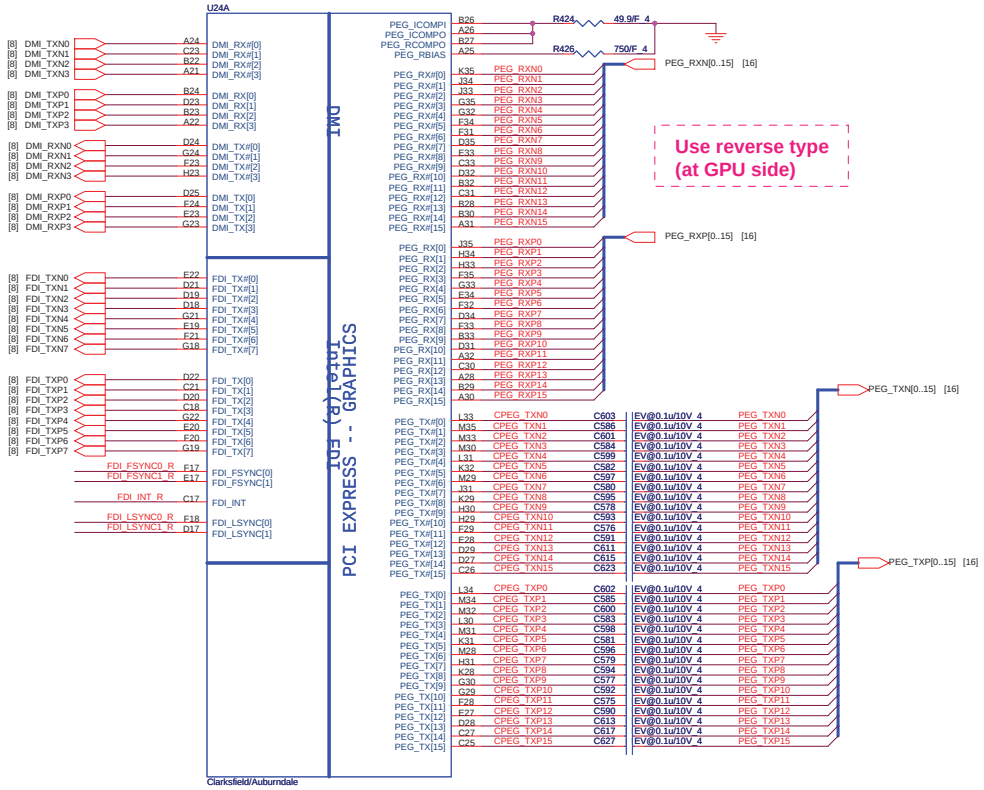
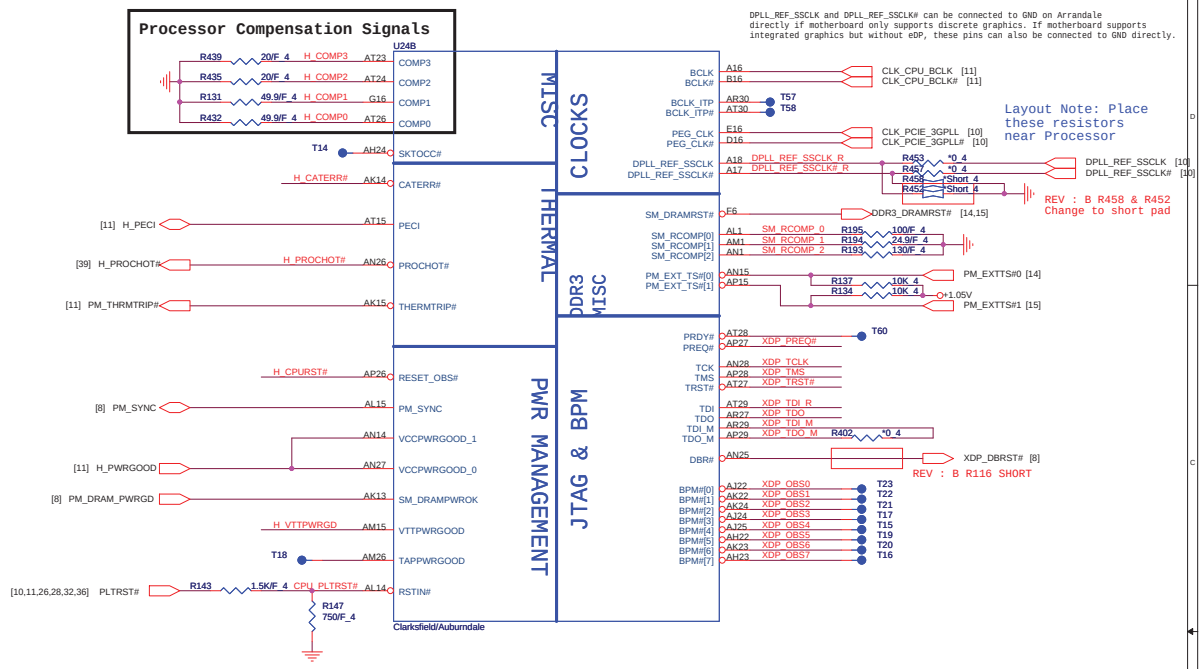
# AUBURNDALE/CLARKSFIELD PROCESSOR (DMI,PEG,FDI)

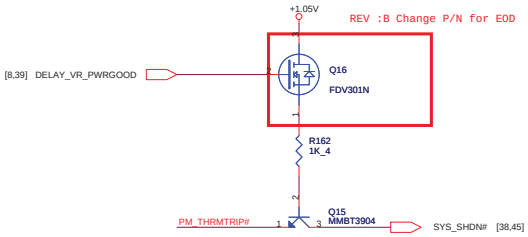



# AUBURNDALE/CLARKSFIELD PROCESSOR (CLK,MISC,JTAG)

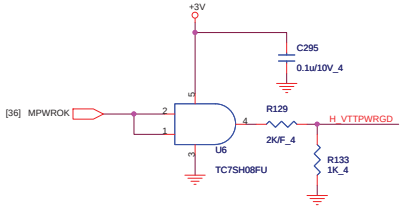



| | |
|---|---|
| LTS | DGG^9000005 |
| SUY | DGG^9000016 |
| FOX | DGG^9000023 |

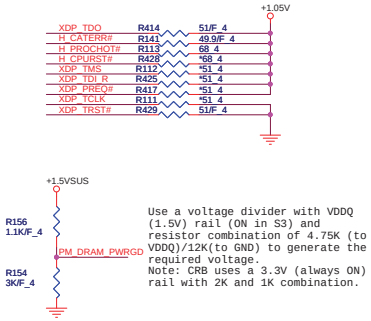
## Thermaltrip protect



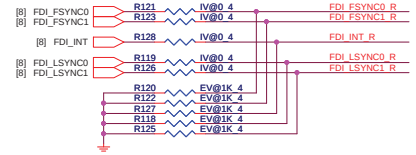

## VTT PWR_Good




## Processor pull-up




Use a voltage divider with VDDQ (1.5V) rail (ON in S3) and resistor combination of 4.75K (to VDDQ)/12K(to GND) to generate the required voltage.
Note: CRB uses a 3.3V (always ON) rail with 2K and 1K combination.




<The GFX_IMON, FDI_FSYNC[0], FDI_FSYNC[1], FDI_LSYNC[0], FDI_LSYNC[1], and FDI_INT>Note that if these signals are left as no connect, there are no functional impacts, but a small amount of power (~15 mW) maybe wasted.

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|---|---|---|
| | AUBURNDA 1/4 | 1C |

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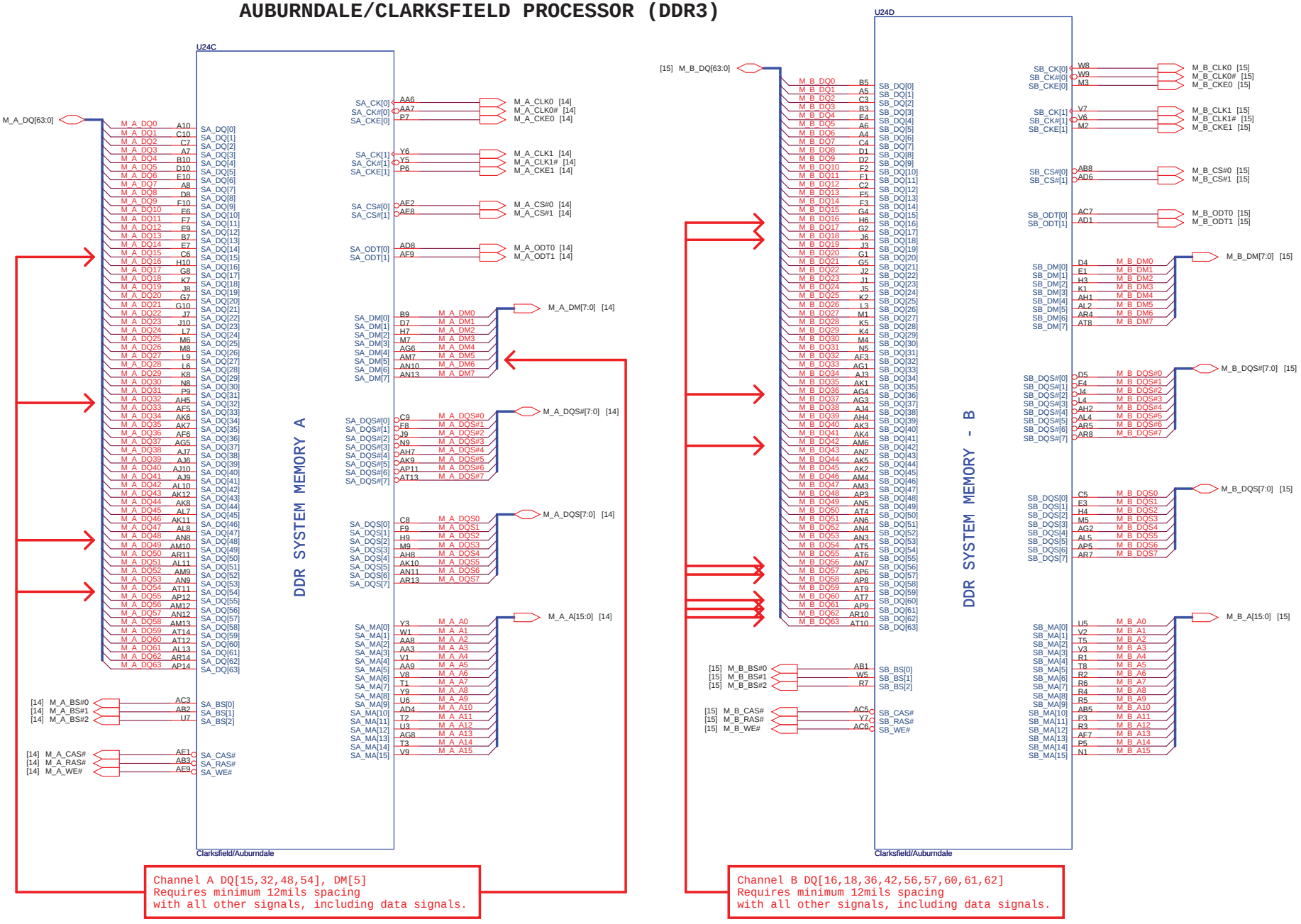
# AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)

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| | AUBURNDA 2/4 | | 1C |
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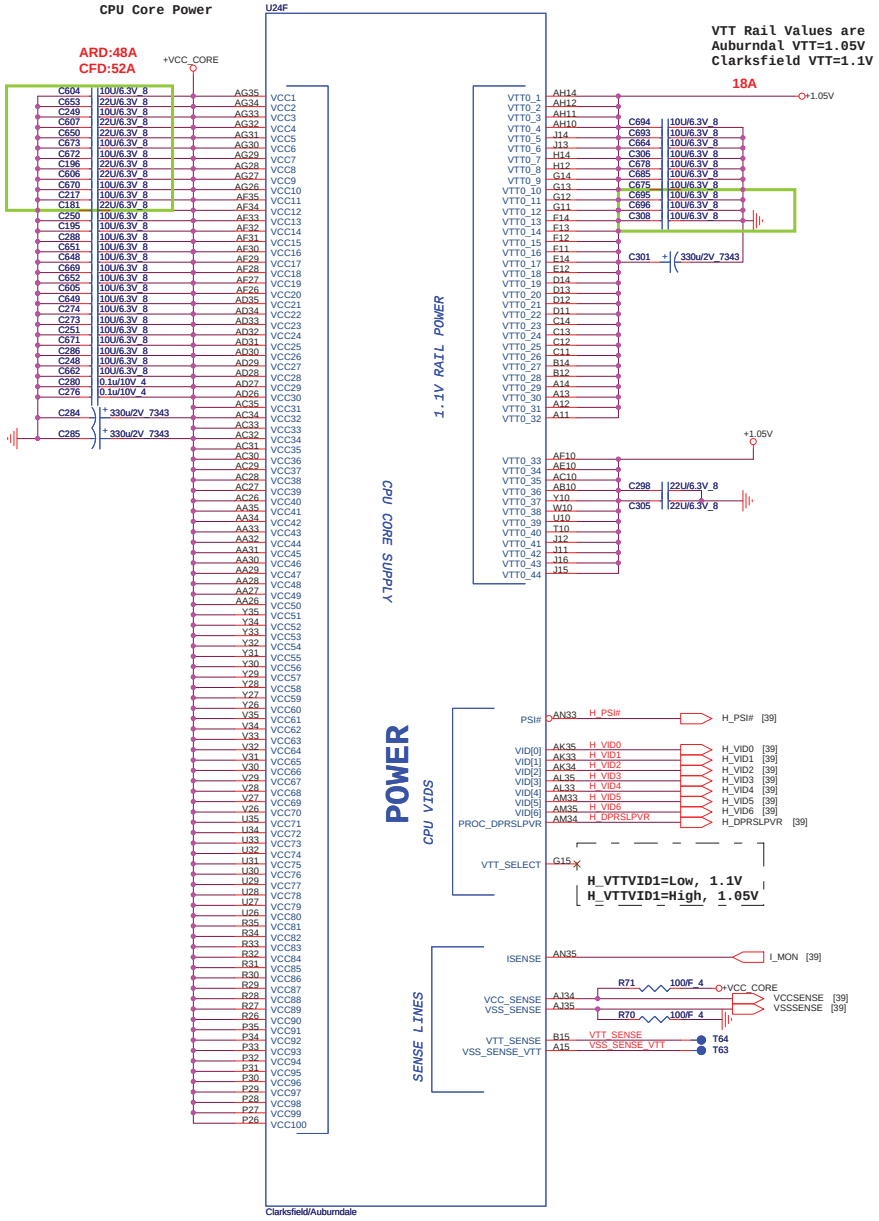
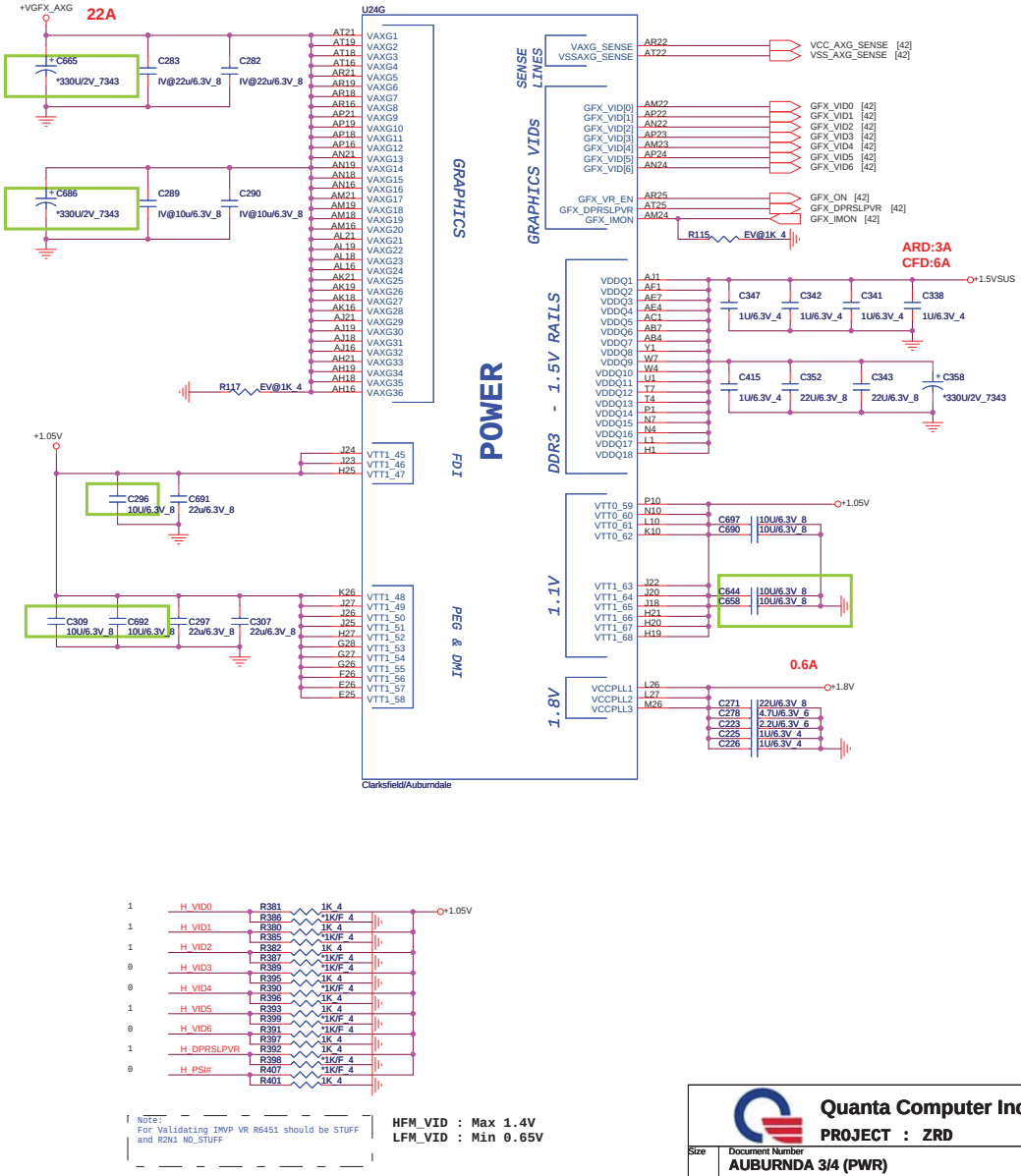



# AUBURNDALE/CLARKSFIELD PROCESSOR (POWER)







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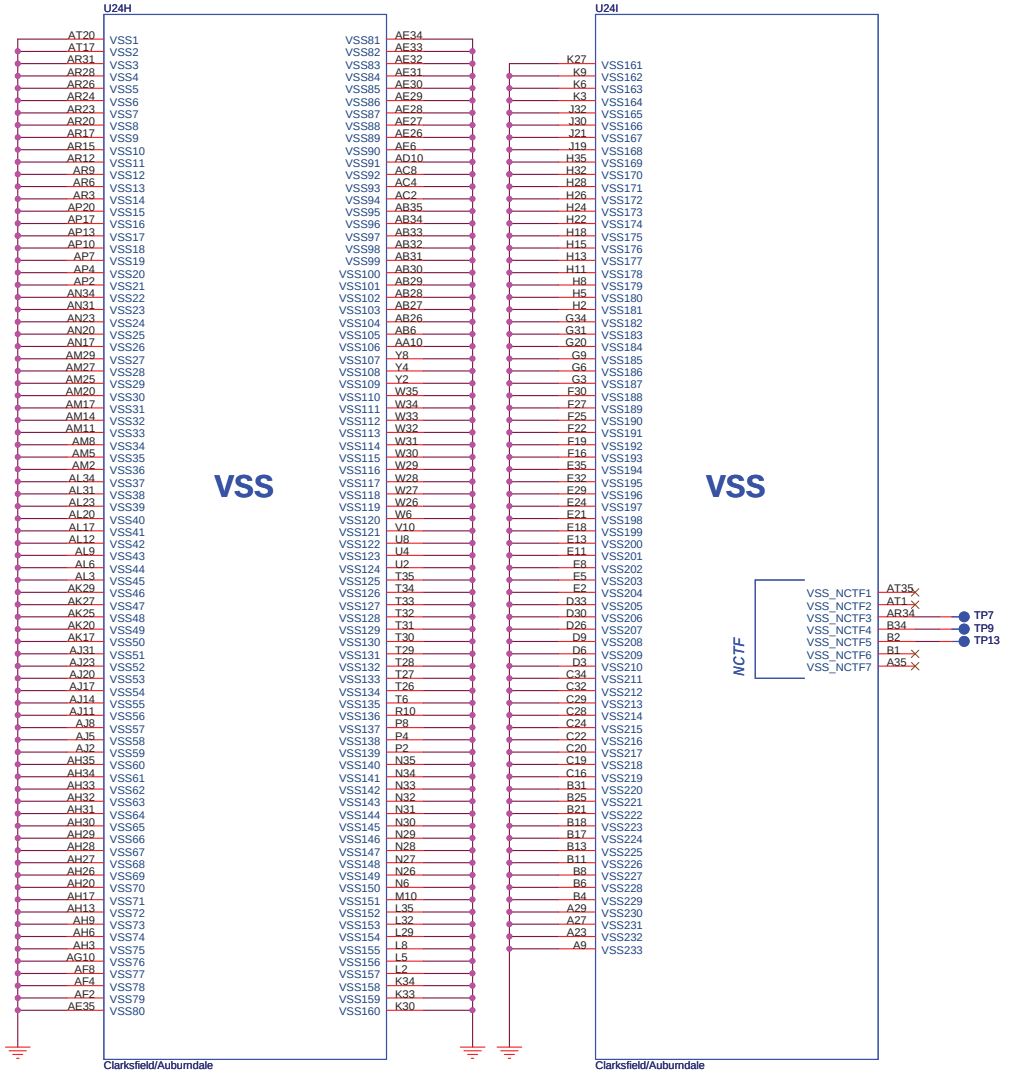
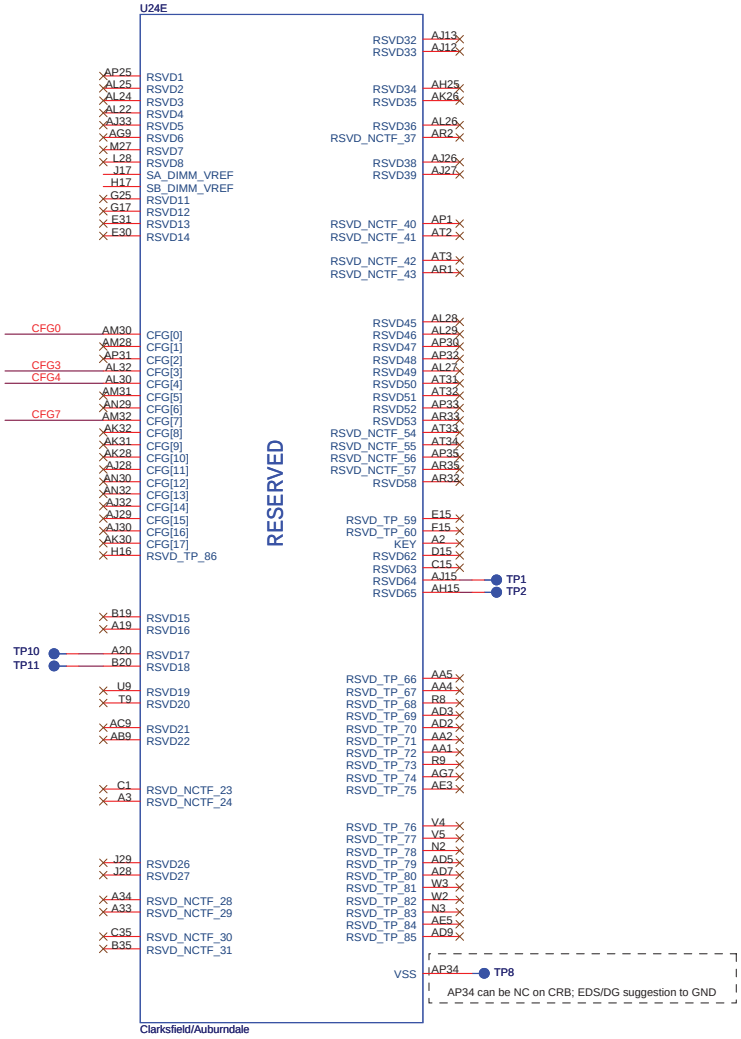
# AUBURNDALE/CLARKSFIELD PROCESSOR (GND)




# AUBURNDALE/CLARKSFIELD PROCESSOR( RESERVED, CFG)




## Processor Strapping

| | 1 | 0 | DEFAULT | |
|---|---|---|---|---|
| CFG0 (PCI-Epress Configuration Select) | Single PEG | Bifurcation enabled | 1 | CFG0 R110 *3.01K_NC |
| CFG3 (PCI-Epress Static Lane Reversal) | Normal Operation | Lane Numbers Reversed | 1 | CFG3 R102 3.01K/F_4 |
| CFG4 (Embended Display Port Presence) | Disabled; No Physical Display Port attached to Embedded Diplay Port | Enabled; An external Display port device is connected to the Embedded Display port | 1 | CFG4 R109 *3.01K |
| The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed. | | | | CFG7 R103 *3.01K/F_4 |

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|---|---|---|
| | AUBURNDA 4/4 | 1C |
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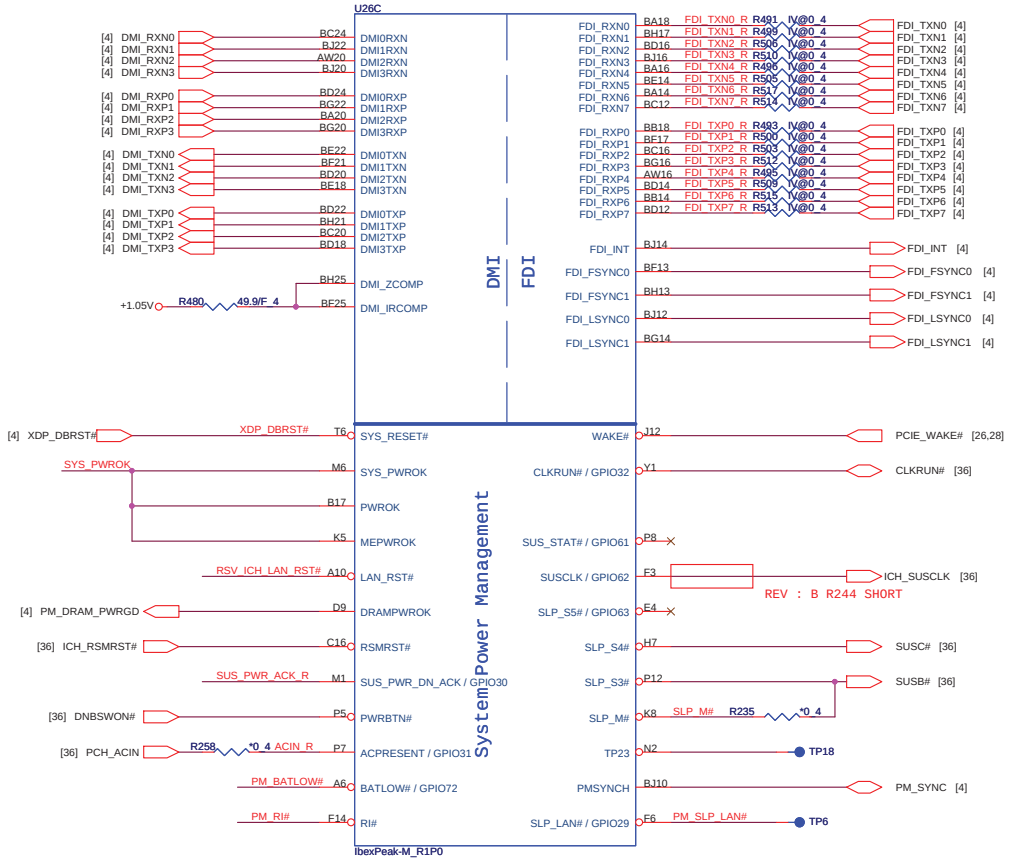
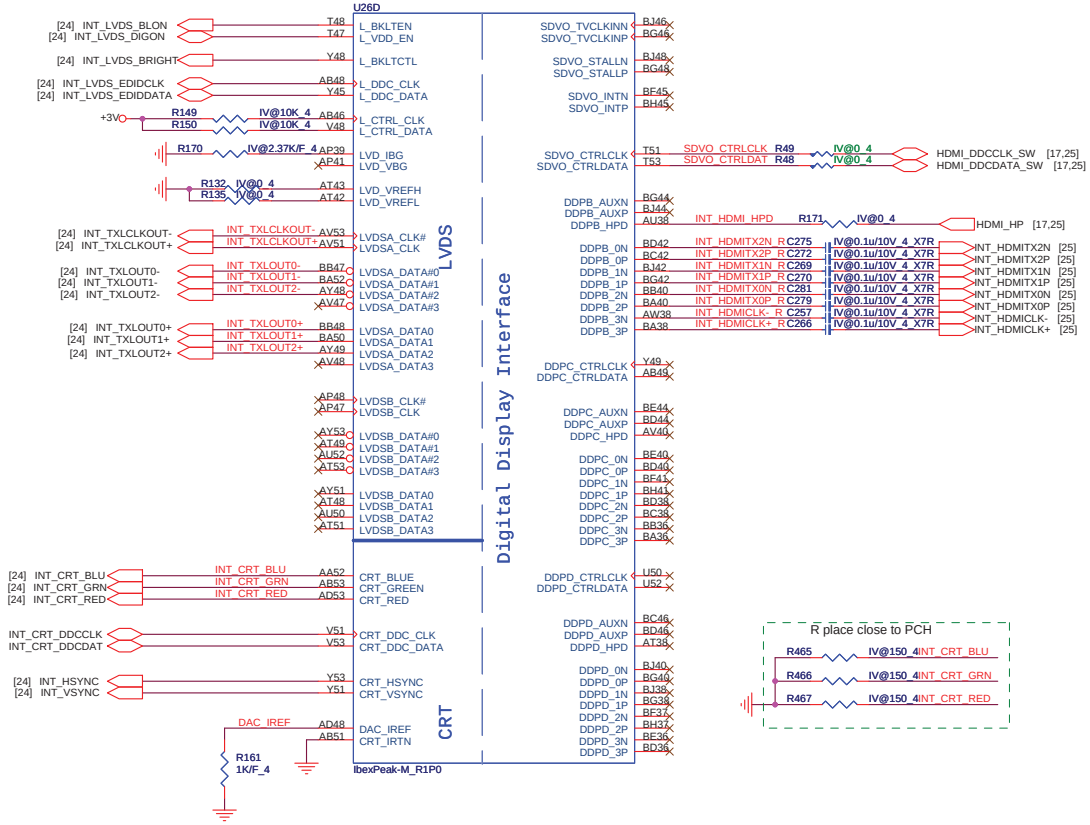
# IBEX PEAK-M (DMI,FDI,GPIO)

0-ohm resistor place close to PCH

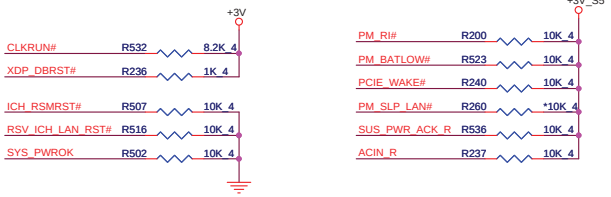



AC-coupling CAP place close to PCH

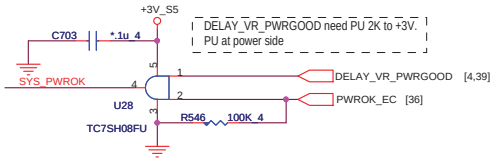
# IBEX PEAK-M (LVDS,DDI)




## PCH Pull-high/low




## System PWR_OK

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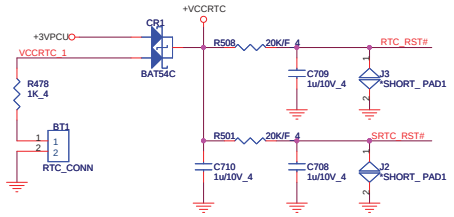
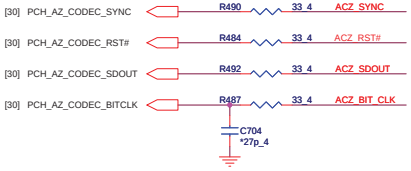
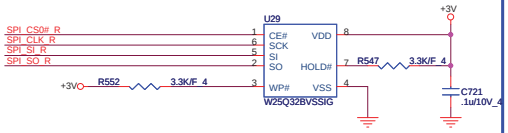
## RTC Circuitry




## HDA Bus

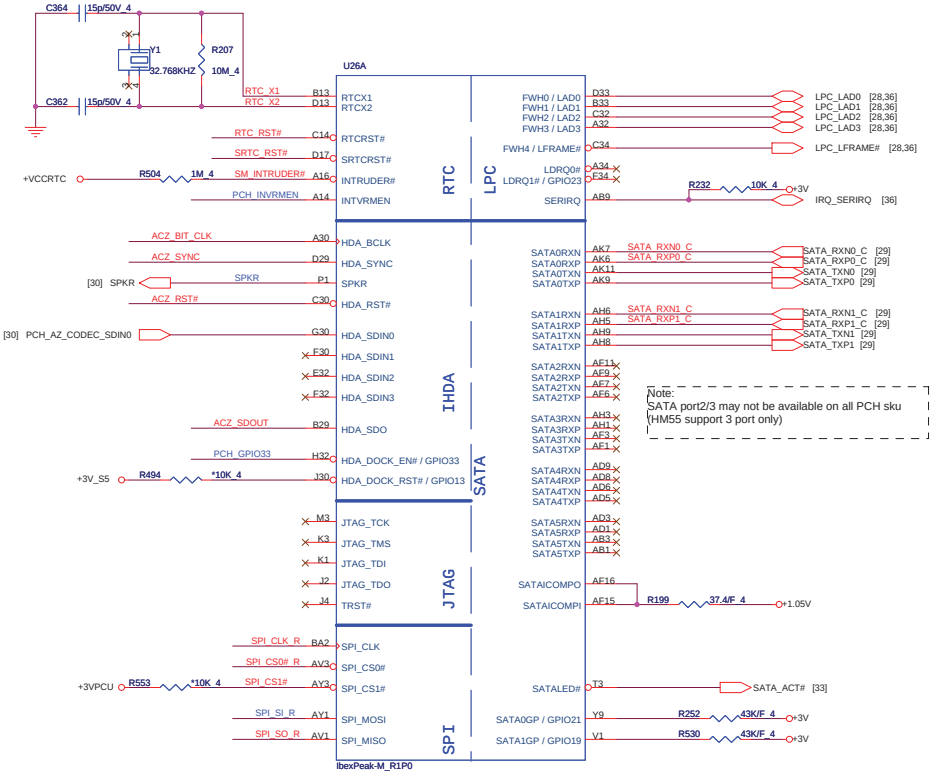



## PCH SPI




**HDA_SYNC (PCH strap pin)**

Internal weak pull-down
VCCVRM=>+1.8V (default)
external pull-up
VCCVRM=>+1.5V




Note:
SATA port2/3 may not be available on all PCH sku (HM55 support 3 port only)

## PCH Strap Pin Configuration Table-1

| | | | |
|---|---|---|---|
| **INTVRMEN** | Integrated 1.05V VRM Enable / Disable | 1 = Integrated VRM is enabled<br>0 = Integrated VRM is disabled | +VCCRTC R511 330K_6 PCH_INVRMEN |
| **SPI_MOSI** | TPM Functionality Disable | 1 = Enabled<br>0 = Disable | +3V R551 *1K_4 SPI_SI_R |
| **SPKR** | Reboot option at power-up | 0 = Default Mode (Internal weak Pull-down)<br>1 = No Reboot Mode with TCO Disabled | +3V R538 *1K/F_4 SPKR |
| **HDA_DOCK_EN #/GPIO33** | Flash Descriptor Security Override | 0 = Flash Descriptor Security will be overridden<br>1 = Security measure defined in the Flash Descriptor will be enabled. | PCH_GPIO33 J1 *SHORT_PAD1 |
| **GNT0#, GNT1#** | Boot BIOS Strap | (0,0) = LPC (0,1) = Reserved NAND<br>(1,0) = PCI (1,1) = SPI | [10] PCI_GNT0# R158 1K_4 R152 1K_4<br>[10] PCI_GNT1# R153 *1K_4 R159 *1K_4 +3V |
| **GNT2#/ GPIO53** | ESI Strap (Server Only) | ESI compatible mode is for server platforms only | [10] PWM_SELECT# R182 *1K/F_4 |
| **GNT3#/ GPIO55** | Top-Block Swap Override | 0 = Top Block Swap Mode<br>1 = Default Mode (Internal pull-up) | [10] PCI_GNT3# R462 *10K/F_4 |
| **NV_ALE** | IntelR Anti-Theft Technology HDD Data Protection (Intel AT-d) Enable | 1 = Enabled<br>0 = Disabled (Default) | [10] NV_ALE R213 *1K/F_4 +1.8V |
| **NV_CLE** | DMI Termination Voltage | DMI termination voltage. Weak internal pull-up. Do not pull low. | [10] NV_CLE R216 *1K/F_4 +1.8V |

| | | | |
|---|---|---|---|
| **GPIO8** | Reserved | This signal has a weak internal pull up.<br>NOTE: This signal should not be pulled low | [11] RSV_GPIO8 R215 10K_4 +3V_S5<br>R214 *1K_4 |
| **GPIO15** | Reserved | 0 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality<br>1 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality | [11] CR_WAKE# R256 1K_4 +3V_S5 |
| **GPIO27** | On-Die PLL Voltage Regulator <internal weak pull-up> | 0 = Disables the VccVRM.<br>1 = Enables the internal VccVRM to have a clean supply for analog rails. | [11] PCH_GPIO27 R231 *10K_4 |

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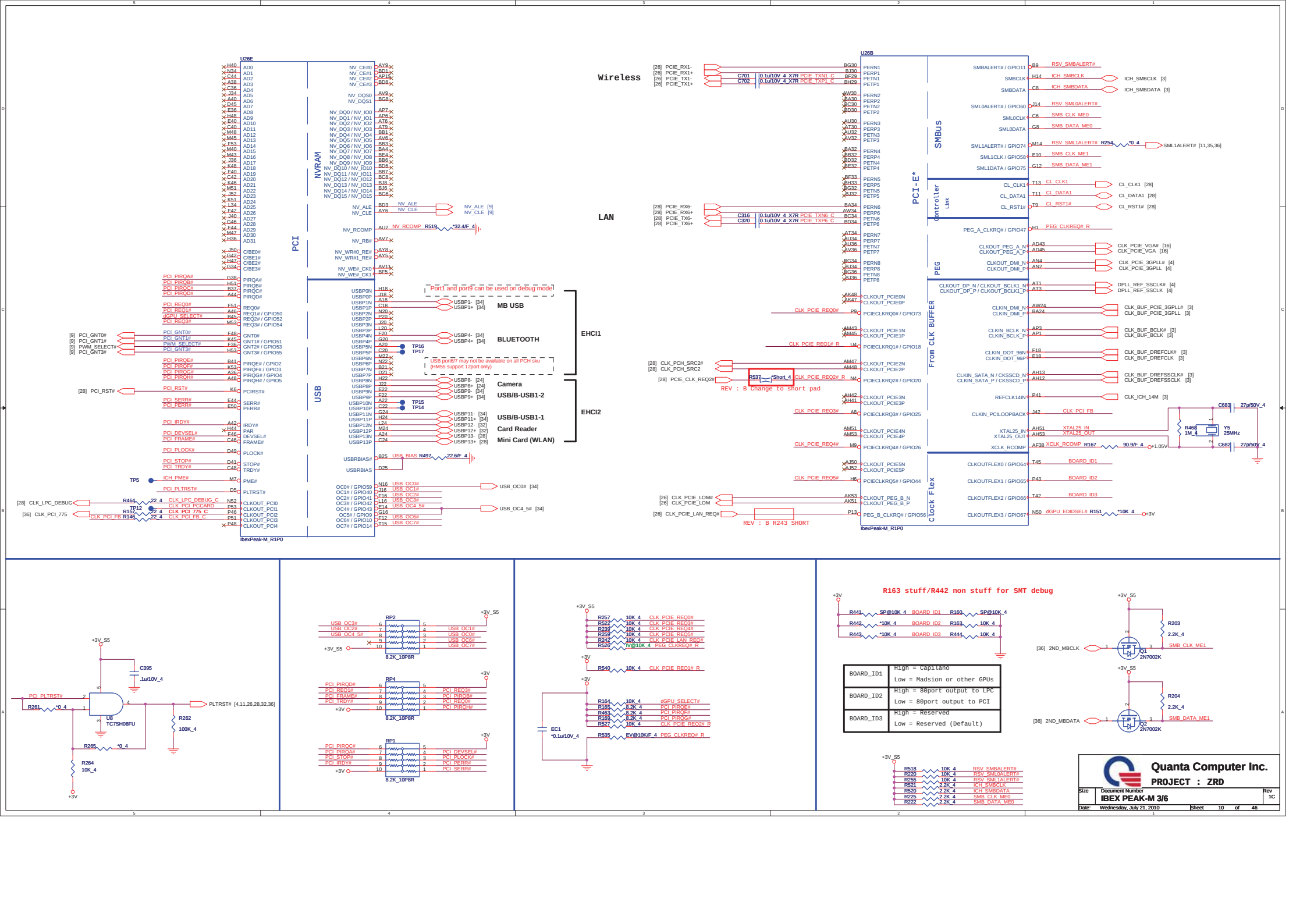
U26E
NVRAM
PCI
USB
IbexPeak-M_R1P0
Port1 and port9 can be used on debug mode
MB USB
BLUETOOTH
Camera
USB/B-USB1-2
USB/B-USB1-1
Card Reader
Mini Card (WLAN)
EHCI1
EHCI2
USB port6/7 may not be available on all PCH sku
(HM55 support 12port only)
U26B
Wireless
LAN
PCI-E*
SMBUs
Controller
Link
PEG
From CLK BUFFER
Clock Flex
REV : B Change to short pad
REV : B R243 SHORT
R163 stuff/R442 non stuff for SMT debug
BOARD_ID1 High = Capitano Low = Madsion or other GPUs
BOARD_ID2 High = 80port output to LPC Low = 80port output to PCI
BOARD_ID3 High = Reserved Low = Reserved (Default)
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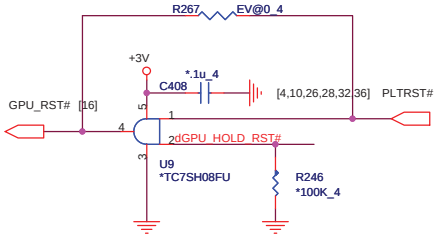
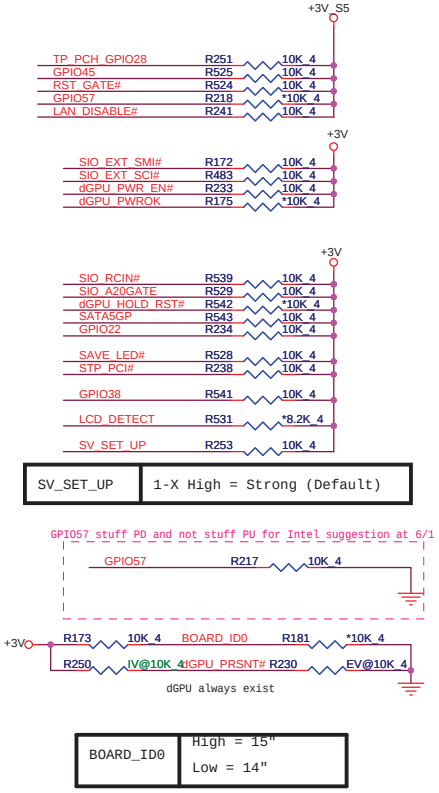
# IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

## GPU RST#




## GPIO Pull-up/Pull-down




| | | |
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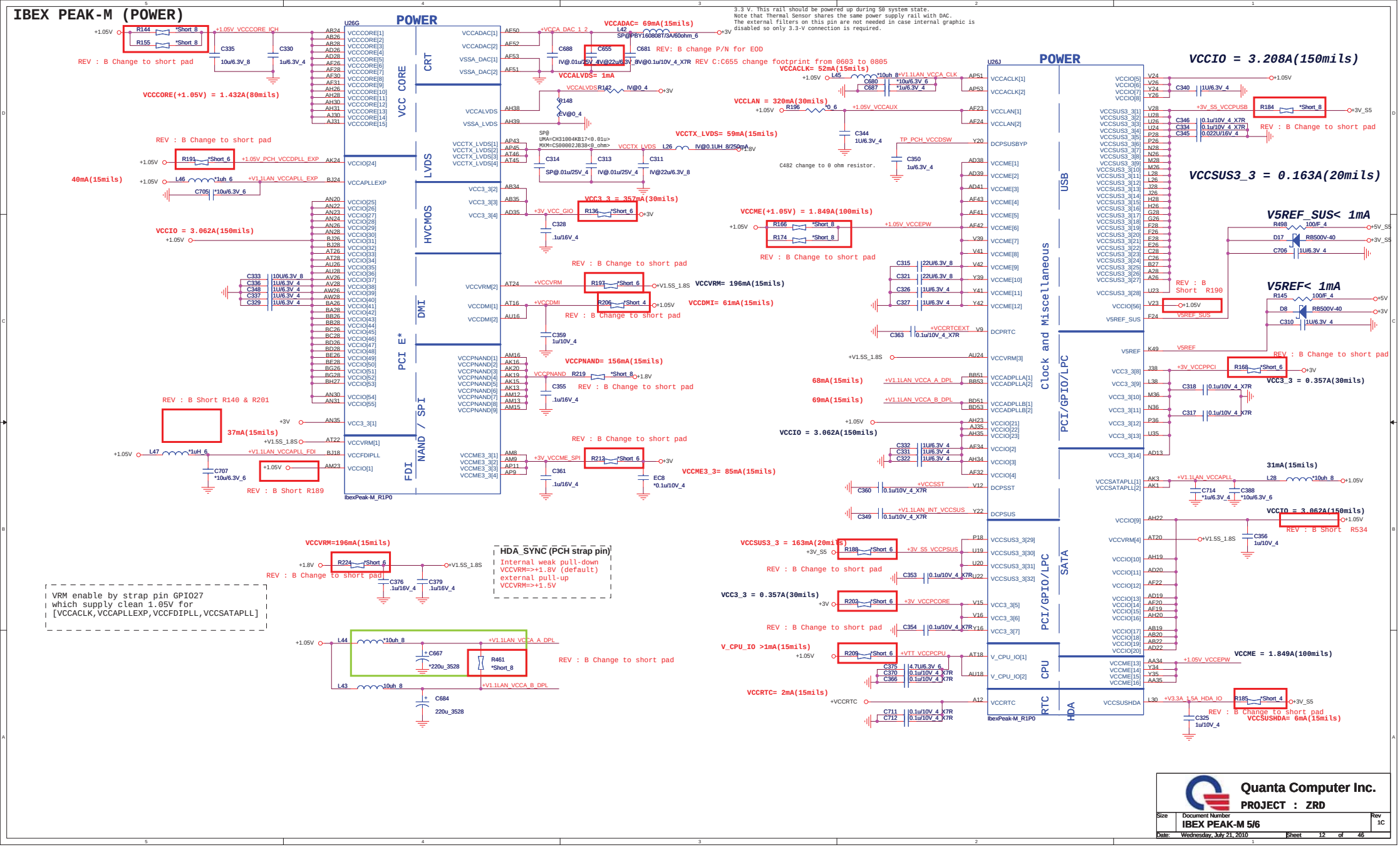
# IBEX PEAK-M (POWER)

3.3 V. This rail should be powered up during S0 system state.
Note that Thermal Sensor shares the same power supply rail with DAC.
The external filters on this pin are not needed in case internal graphic is disabled so only 3.3-V connection is required.

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| Size | Document Number | Rev |
|---|---|---|
| | IBEX PEAK-M 5/6 | 1C |

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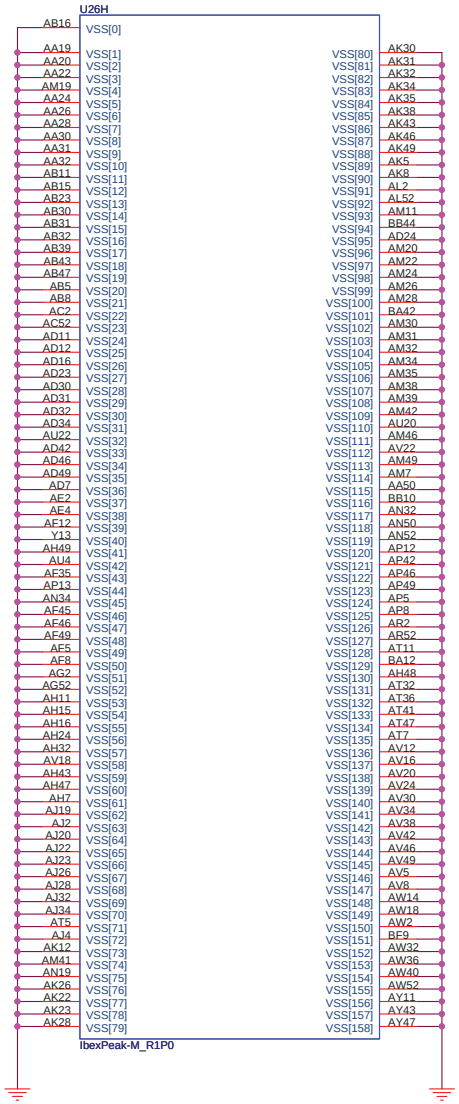
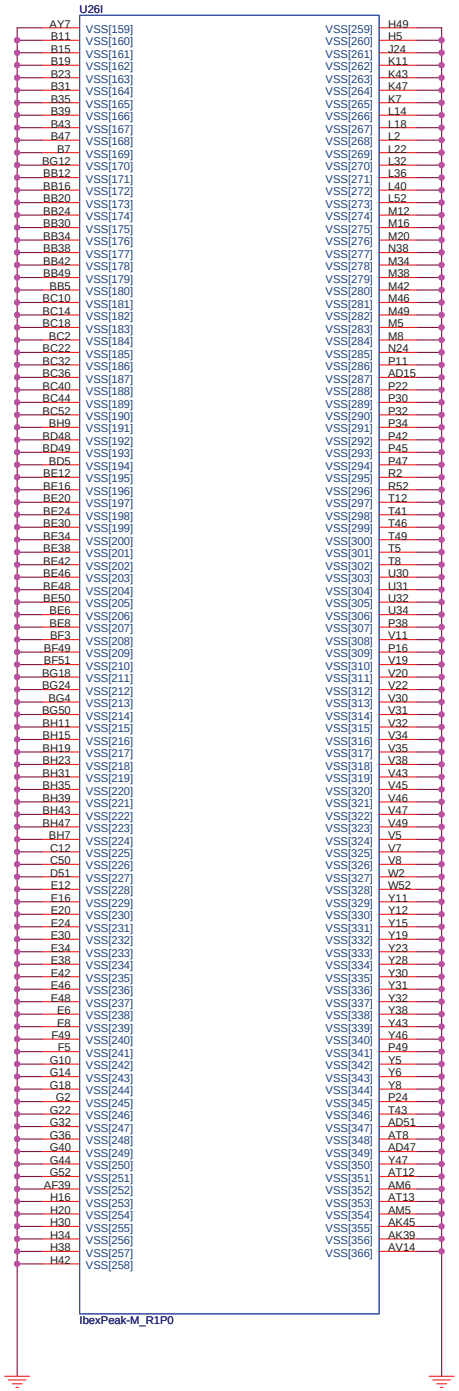
# IBEX PEAK-M (GND)

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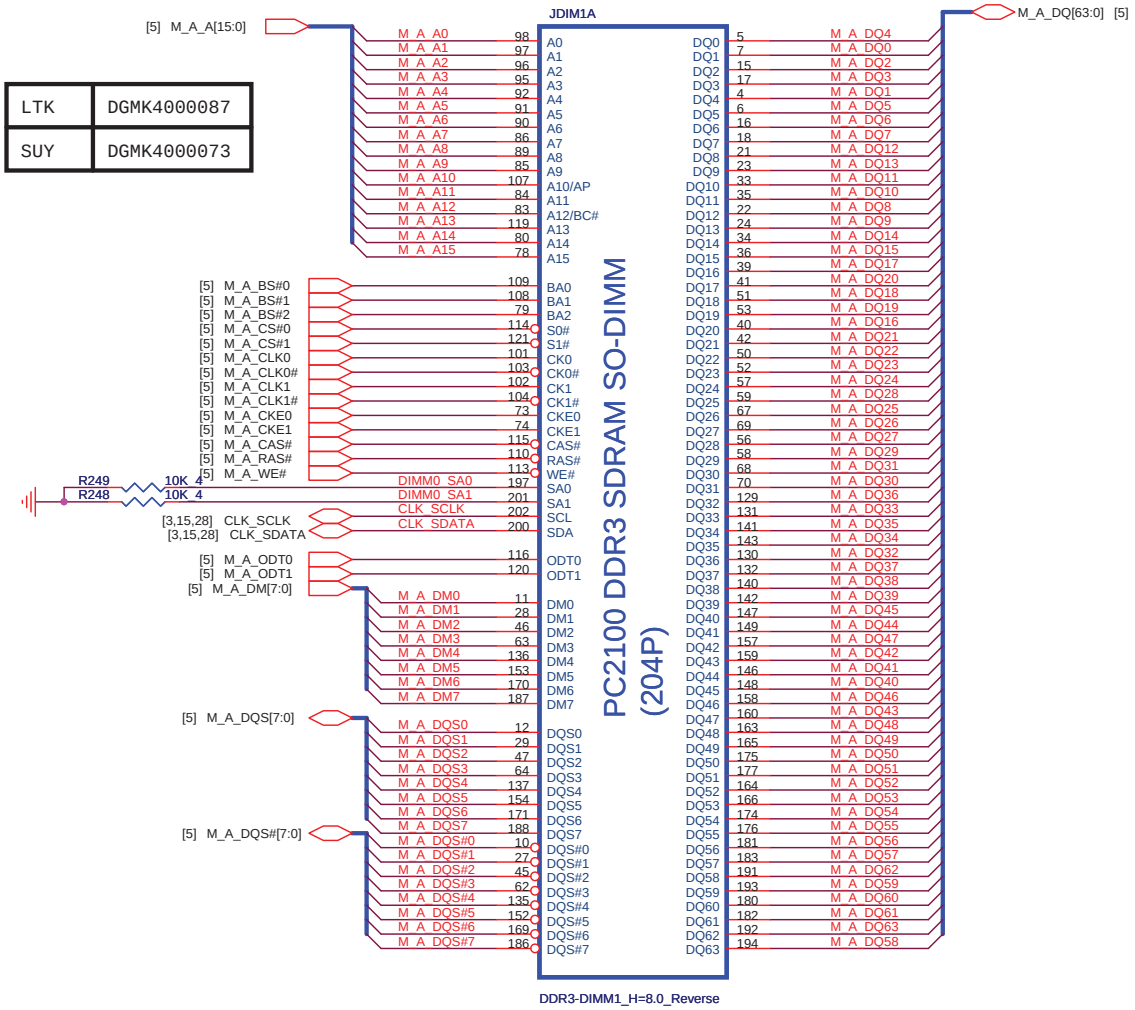
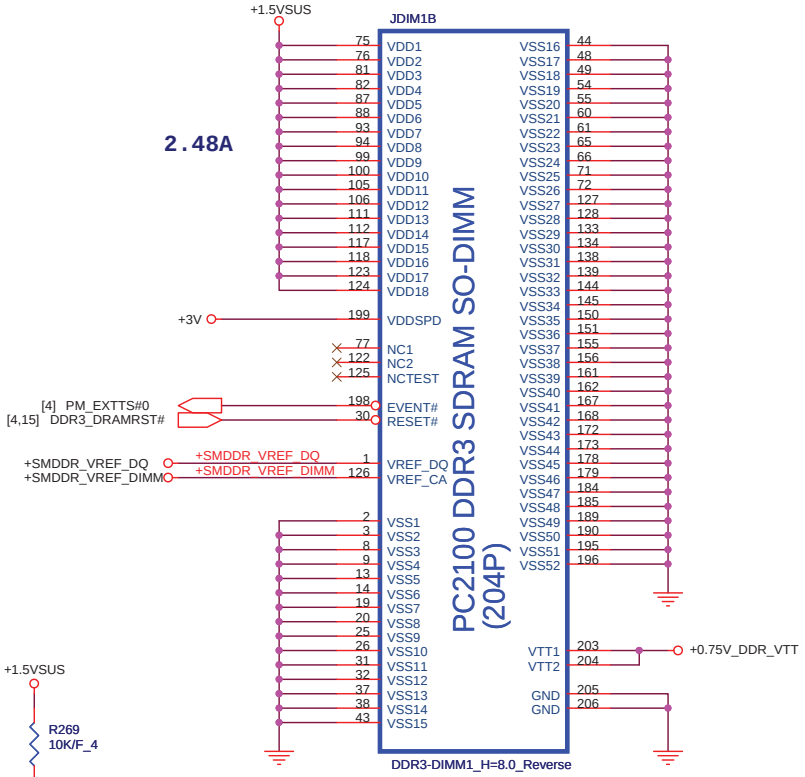
PROJECT : ZRD

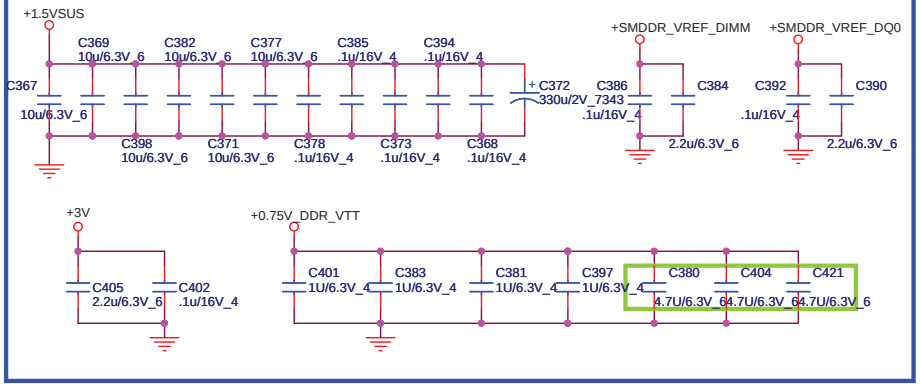
| Size | Document Number | Rev |
|---|---|---|
| | IBEX PEAK-M 6/6 | 1C |
| Date: Wednesday, July 21, 2010 | Sheet 13 of 46 | |

| | |
|---|---|
| LTK | DGMK4000087 |
| SUY | DGMK4000073 |




## Place these Caps near So-Dimm0.

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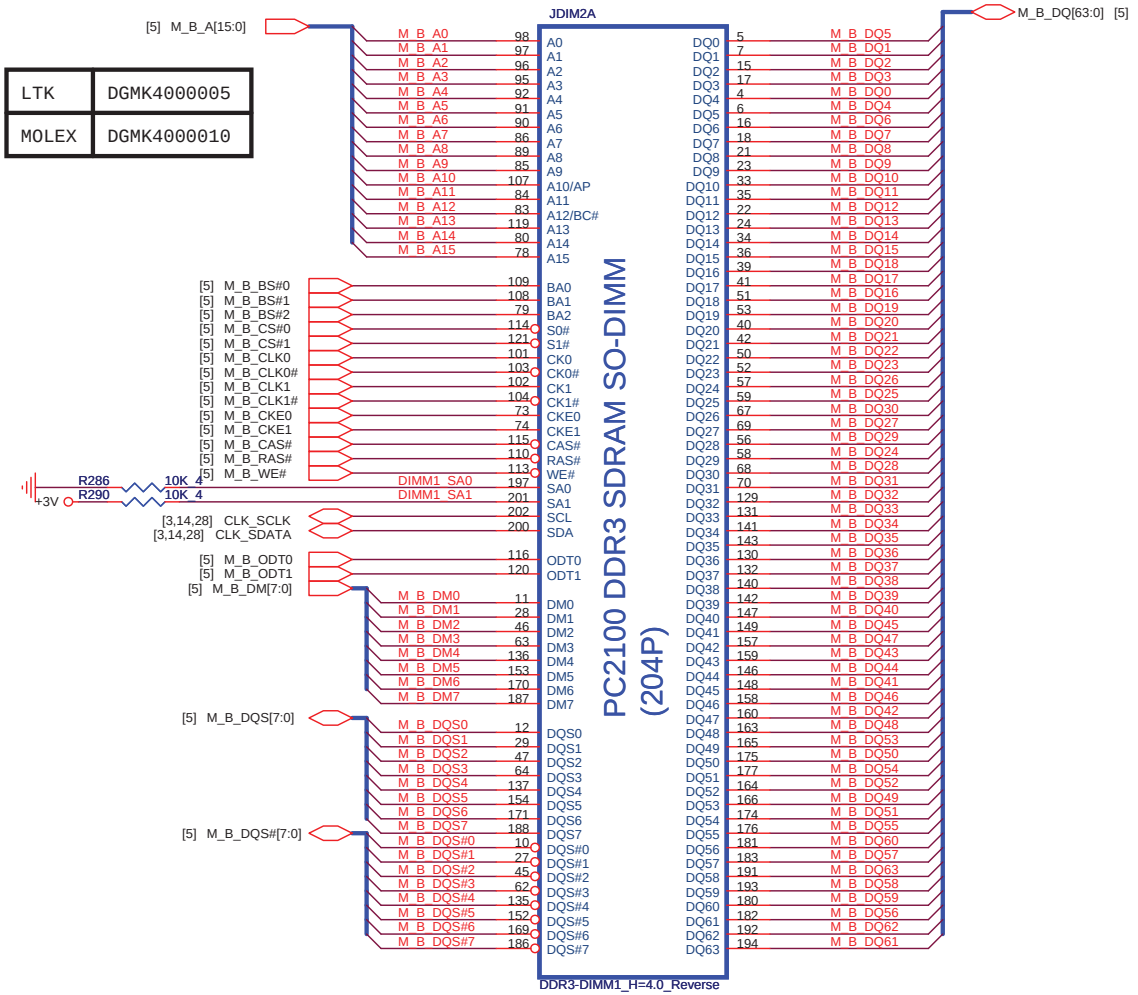
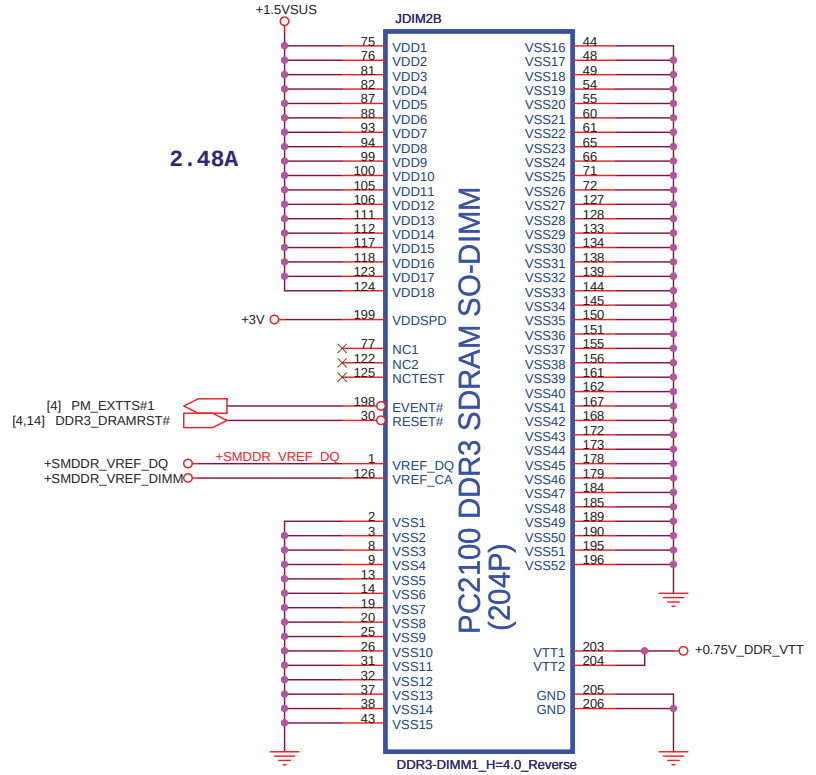
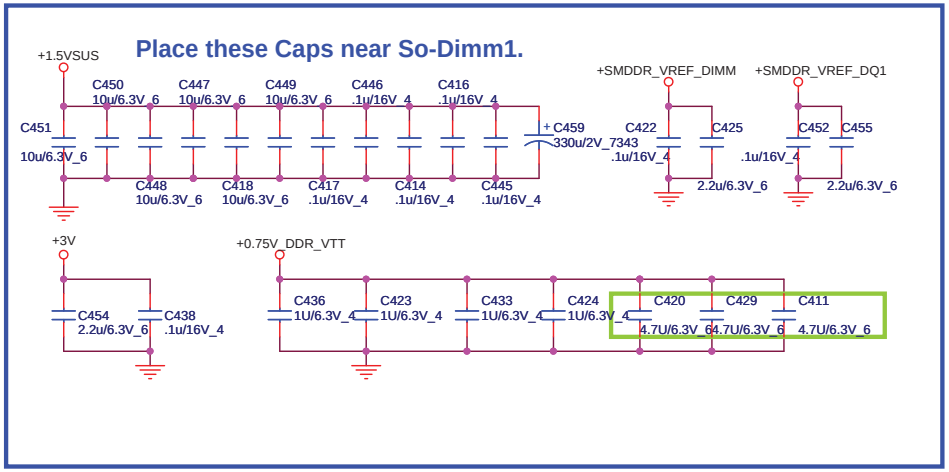
PROJECT : ZRD

| Size | Document Number | Rev |
|---|---|---|
| | DDRIII SO-DIMM-0 | 1C |
| Date: | Wednesday, July 21, 2010 | Sheet 14 of 46 |

| | |
|---|---|
| LTK | DGMK4000005 |
| MOLEX | DGMK4000010 |

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PROJECT : ZRD

| Size | Document Number | Rev |
|---|---|---|
| | DDRIII SO-DIMM-1 | 1C |
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# GPU_1(VGA)

[4] PEG_TXP[0..15] PEG_TXP[0..15]
[4] PEG_TXN[0..15] PEG_TXN[0..15]
[4] PEG_RXP[0..15] PEG_RXP[0..15]
[4] PEG_RXN[0..15] PEG_RXN[0..15]

U21A

0518 SWAP PCIE for VGA side

| | | | | |
|---|---|---|---|---|
| [4] PEG_TXP15 | PEG_TXP15 | AA38 | PCIE_RX0P | |
| [4] PEG_TXN15 | PEG_TXN15 | Y37 | PCIE_RX0N | |
| [4] PEG_TXP14 | PEG_TXP14 | Y35 | PCIE_RX1P | |
| [4] PEG_TXN14 | PEG_TXN14 | W36 | PCIE_RX1N | |
| [4] PEG_TXP13 | PEG_TXP13 | W38 | PCIE_RX2P | |
| [4] PEG_TXN13 | PEG_TXN13 | V37 | PCIE_RX2N | |
| [4] PEG_TXP12 | PEG_TXP12 | V35 | PCIE_RX3P | |
| [4] PEG_TXN12 | PEG_TXN12 | U36 | PCIE_RX3N | |
| [4] PEG_TXP11 | PEG_TXP11 | U38 | PCIE_RX4P | |
| [4] PEG_TXN11 | PEG_TXN11 | T37 | PCIE_RX4N | |
| [4] PEG_TXP10 | PEG_TXP10 | T35 | PCIE_RX5P | |
| [4] PEG_TXN10 | PEG_TXN10 | R36 | PCIE_RX5N | |
| [4] PEG_TXP9 | PEG_TXP9 | R38 | PCIE_RX6P | |
| [4] PEG_TXN9 | PEG_TXN9 | P37 | PCIE_RX6N | |
| [4] PEG_TXP8 | PEG_TXP8 | P35 | PCIE_RX7P | |
| [4] PEG_TXN8 | PEG_TXN8 | N36 | PCIE_RX7N | |
| [4] PEG_TXP7 | PEG_TXP7 | N38 | PCIE_RX8P | |
| [4] PEG_TXN7 | PEG_TXN7 | M37 | PCIE_RX8N | |
| [4] PEG_TXP6 | PEG_TXP6 | M35 | PCIE_RX9P | |
| [4] PEG_TXN6 | PEG_TXN6 | L36 | PCIE_RX9N | |
| [4] PEG_TXP5 | PEG_TXP5 | L38 | PCIE_RX10P | |
| [4] PEG_TXN5 | PEG_TXN5 | K37 | PCIE_RX10N | |
| [4] PEG_TXP4 | PEG_TXP4 | K35 | PCIE_RX11P | |
| [4] PEG_TXN4 | PEG_TXN4 | J36 | PCIE_RX11N | |
| [4] PEG_TXP3 | PEG_TXP3 | J38 | PCIE_RX12P | |
| [4] PEG_TXN3 | PEG_TXN3 | H37 | PCIE_RX12N | |
| [4] PEG_TXP2 | PEG_TXP2 | H35 | PCIE_RX13P | |
| [4] PEG_TXN2 | PEG_TXN2 | G36 | PCIE_RX13N | |
| [4] PEG_TXP1 | PEG_TXP1 | G38 | PCIE_RX14P | |
| [4] PEG_TXN1 | PEG_TXN1 | F37 | PCIE_RX14N | |
| [4] PEG_TXP0 | PEG_TXP0 | F35 | PCIE_RX15P | |
| [4] PEG_TXN0 | PEG_TXN0 | E37 | PCIE_RX15N | |

PCI EXPRESS INTERFACE

0518 SWAP PCIE for VGA side

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| PCIE_TX0P | Y33 | CPEG_RXP15 | C155 | EV@0.1u/10V_4 | PEG_RXP15 [4] |
| PCIE_TX0N | Y32 | CPEG_RXN15 | C164 | EV@0.1u/10V_4 | PEG_RXN15 [4] |
| PCIE_TX1P | W33 | CPEG_RXP14 | C147 | EV@0.1u/10V_4 | PEG_RXP14 [4] |
| PCIE_TX1N | W32 | CPEG_RXN14 | C154 | EV@0.1u/10V_4 | PEG_RXN14 [4] |
| PCIE_TX2P | U33 | CPEG_RXP13 | C141 | EV@0.1u/10V_4 | PEG_RXP13 [4] |
| PCIE_TX2N | U32 | CPEG_RXN13 | C146 | EV@0.1u/10V_4 | PEG_RXN13 [4] |
| PCIE_TX3P | U30 | CPEG_RXP12 | C136 | EV@0.1u/10V_4 | PEG_RXP12 [4] |
| PCIE_TX3N | U29 | CPEG_RXN12 | C131 | EV@0.1u/10V_4 | PEG_RXN12 [4] |
| PCIE_TX4P | T33 | CPEG_RXP11 | C130 | EV@0.1u/10V_4 | PEG_RXP11 [4] |
| PCIE_TX4N | T32 | CPEG_RXN11 | C116 | EV@0.1u/10V_4 | PEG_RXN11 [4] |
| PCIE_TX5P | T30 | CPEG_RXP10 | C109 | EV@0.1u/10V_4 | PEG_RXP10 [4] |
| PCIE_TX5N | T29 | CPEG_RXN10 | C106 | EV@0.1u/10V_4 | PEG_RXN10 [4] |
| PCIE_TX6P | P33 | CPEG_RXP9 | C105 | EV@0.1u/10V_4 | PEG_RXP9 [4] |
| PCIE_TX6N | P32 | CPEG_RXN9 | C92 | EV@0.1u/10V_4 | PEG_RXN9 [4] |
| PCIE_TX7P | P30 | CPEG_RXP8 | C91 | EV@0.1u/10V_4 | PEG_RXP8 [4] |
| PCIE_TX7N | P29 | CPEG_RXN8 | C87 | EV@0.1u/10V_4 | PEG_RXN8 [4] |
| PCIE_TX8P | N33 | CPEG_RXP7 | C86 | EV@0.1u/10V_4 | PEG_RXP7 [4] |
| PCIE_TX8N | N32 | CPEG_RXN7 | C80 | EV@0.1u/10V_4 | PEG_RXN7 [4] |
| PCIE_TX9P | N30 | CPEG_RXP6 | C79 | EV@0.1u/10V_4 | PEG_RXP6 [4] |
| PCIE_TX9N | N29 | CPEG_RXN6 | C75 | EV@0.1u/10V_4 | PEG_RXN6 [4] |
| PCIE_TX10P | L33 | CPEG_RXP5 | C72 | EV@0.1u/10V_4 | PEG_RXP5 [4] |
| PCIE_TX10N | L32 | CPEG_RXN5 | C69 | EV@0.1u/10V_4 | PEG_RXN5 [4] |
| PCIE_TX11P | L30 | CPEG_RXP4 | C67 | EV@0.1u/10V_4 | PEG_RXP4 [4] |
| PCIE_TX11N | L29 | CPEG_RXN4 | C63 | EV@0.1u/10V_4 | PEG_RXN4 [4] |
| PCIE_TX12P | K33 | CPEG_RXP3 | C59 | EV@0.1u/10V_4 | PEG_RXP3 [4] |
| PCIE_TX12N | K32 | CPEG_RXN3 | C61 | EV@0.1u/10V_4 | PEG_RXN3 [4] |
| PCIE_TX13P | J33 | CPEG_RXP2 | C56 | EV@0.1u/10V_4 | PEG_RXP2 [4] |
| PCIE_TX13N | J32 | CPEG_RXN2 | C58 | EV@0.1u/10V_4 | PEG_RXN2 [4] |
| PCIE_TX14P | K30 | CPEG_RXP1 | C50 | EV@0.1u/10V_4 | PEG_RXP1 [4] |
| PCIE_TX14N | K29 | CPEG_RXN1 | C48 | EV@0.1u/10V_4 | PEG_RXN1 [4] |
| PCIE_TX15P | H33 | CPEG_RXP0 | C55 | EV@0.1u/10V_4 | PEG_RXP0 [4] |
| PCIE_TX15N | H32 | CPEG_RXN0 | C52 | EV@0.1u/10V_4 | PEG_RXN0 [4] |

CLOCK

[10] CLK_PCIE_VGA AB35 PCIE_REFCLKP
[10] CLK_PCIE_VGA# AA36 PCIE_REFCLKN

For Broadway, Madison and Park
the PWRGOOD ball must be connecctd to ground

R67 EV@10K_4

AJ21 NC#1
AK21 NC#2
AH16 PWRGOOD

[11] GPU_RST# AA30 PERSTB

SP@Capilano/Robson

CALIBRATION

PCIE_CALRP Y30 R47 EV@1.27K/F_4
PCIE_CALRN Y29 R46 EV@2K/F_4 +1V

**+1.0V**

For M97, Broadway, Madison and Park PCIE_VDDC is 1.0V

| | |
|---|---|
| Madison | AJ007720T02 |
| Park | AJ077400T08 |

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| Size | Document Number | Rev |
|---|---|---|
| | Capilano/Robson -PCIE I/F | 1C |
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# GPU_2(VGA)

## GPU Power-on sequence

1 => +VGPU_CORE
2 => +VGPU_IO
3 => +1V
4 => +1.5V_GPU
5 => +3V_D
6 => +1.8V_GPU
7 => dGPU_PWROK

1.8V GPIO

3.3V GPIO

NC on Park

NC on Park

Channel D N.C for Park-M2

DAC2 will be NC on future ASIC

REV C: C188 change footprint from 0603 to 0805

HDMI

DDC AUX4 NC for Park_M2

LVDS

CRT

DDC AUX7 NC for Park_M2

SP@Capilano/Robson

SP@Capilano/Robson

| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT : ZRD | | |
| Size | Document Number: Capilano/Robson -PCIE I/F | Rev: 1C |
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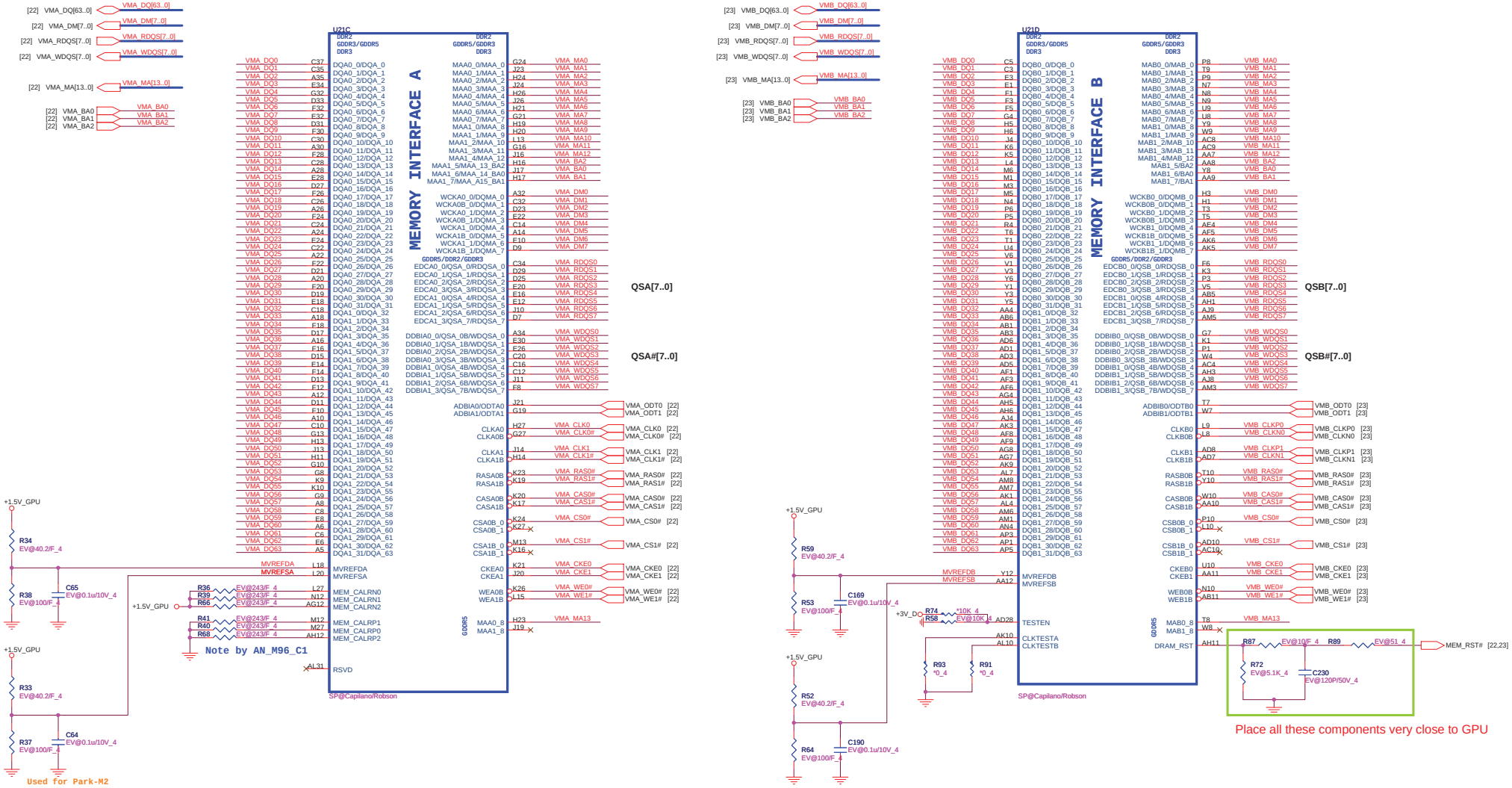
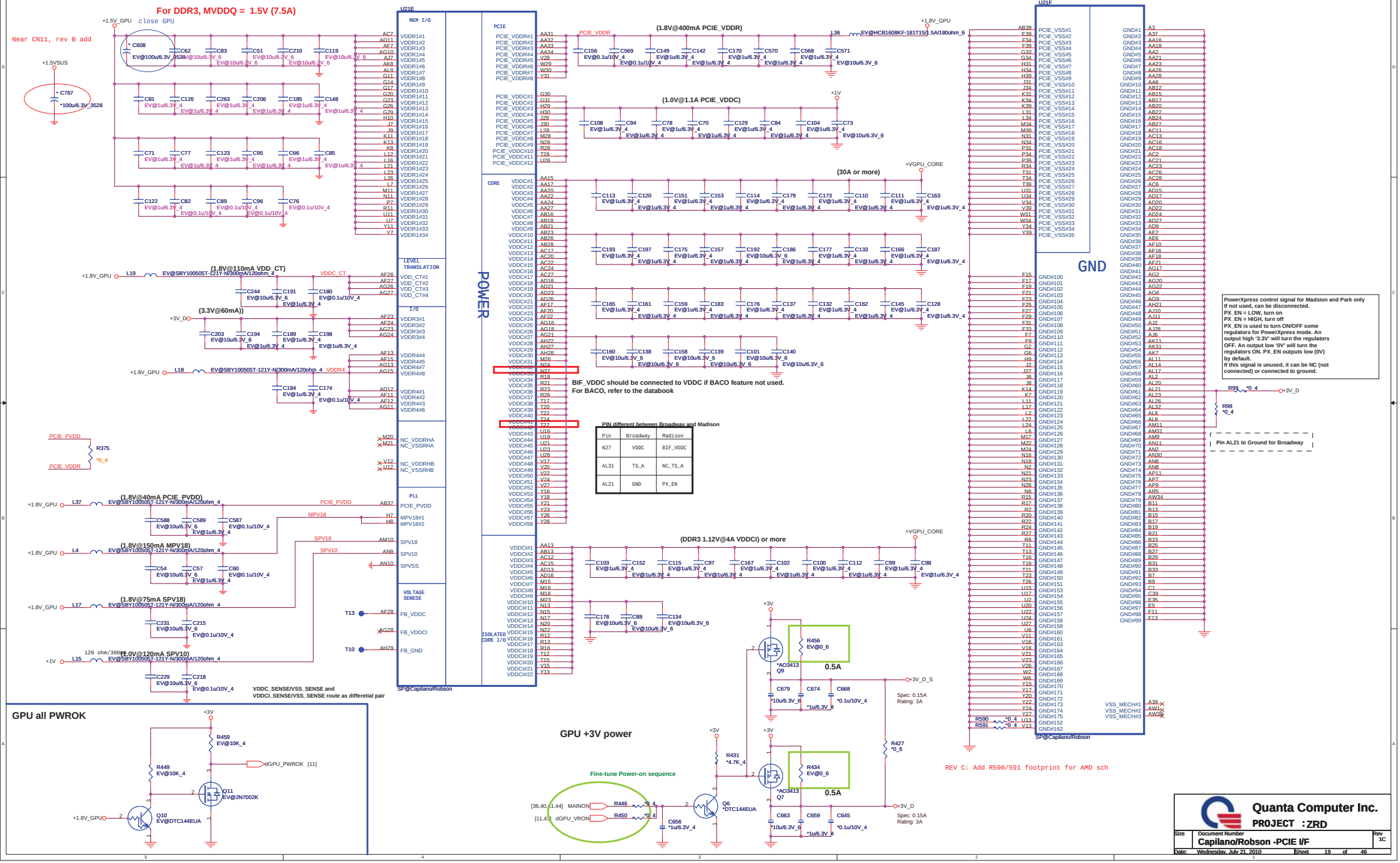
# GPU_3(VGA)

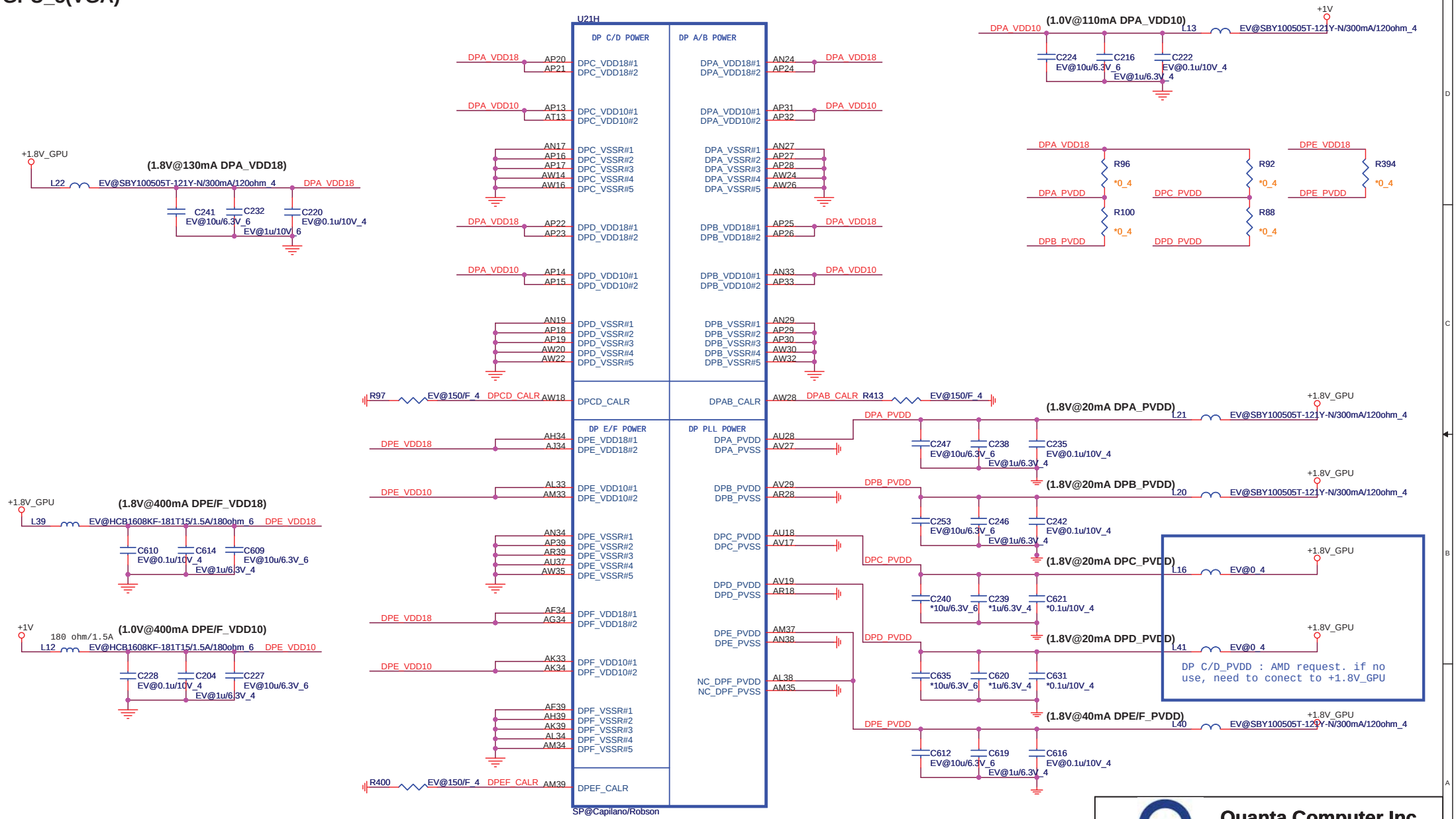
Park M2-channel B used(S3 package use Channel A)



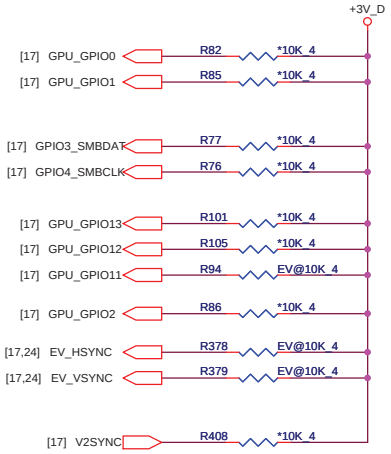
# GPU_4(VGA)


For DDR3, MVDDQ = 1.5V (7.5A)
U21E
MEM I/O
POWER
LEVEL TRANSLATION
I/O
PLL
VOLTAGE SENSE
SP@Capilano/Robson
(1.8V@400mA PCIE_VDDR)
(1.0V@1.1A PCIE_VDDC)
(30A or more)
(DDR3 1.12V@4A VDDCI) or more
(1.8V@110mA VDD_CT)
(3.3V@60mA))
(1.8V@40mA PCIE_PVDD)
(1.8V@150mA MPV18)
(1.8V@75mA SPV18)
(1.0V@120mA SPV10)
BIF_VDDC should be connected to VDDC if BACO feature not used.
For BACO, refer to the databook
PIN different between Broadway and Madison
Pin | Broadway | Madison
N27 | VDDC | BIF_VDDC
AL31 | TS_A | NC_TS_A
AL21 | GND | PX_EN
U21F
GND
PowerXpress control signal for Madsion and Park only
If not used, can be disconnected.
PX_EN = LOW, turn on
PX_EN = HIGH, turn off
PX_EN is used to turn ON/OFF some regulators for PowerXpress mode. An output high '3.3V' will turn the regulators OFF. An output low '0V' will turn the regulators ON. PX_EN outputs low (0V) by default.
If this signal is unused, it can be NC (not connected) or connected to ground.
Pin AL21 to Ground for Broadway
GPU all PWROK
GPU +3V power
Fine-tune Power-on sequence
REV C: Add R590/591 footprint for AMD sch

# GPU_5(VGA)


U21H
DP C/D POWER
DP A/B POWER
DP E/F POWER
DP PLL POWER
SP@Capilano/Robson
(1.8V@130mA DPA_VDD18)
(1.0V@110mA DPA_VDD10)
(1.8V@20mA DPA_PVDD)
(1.8V@20mA DPB_PVDD)
(1.8V@20mA DPC_PVDD)
(1.8V@20mA DPD_PVDD)
(1.8V@40mA DPE/F_PVDD)
(1.8V@400mA DPE/F_VDD18)
(1.0V@400mA DPE/F_VDD10)
DP C/D_PVDD : AMD request. if no use, need to conect to +1.8V_GPU

## PIN STRAPS(VGA)




| Size of the primary memory apertures | GPIO[13:11] |
|---|---|
| 128 MB | 000 |
| 256MB | 001 |
| 64 MB | 010 |
| 32 MB | 011 |
| More than 512 MB | Not Supported |

## CONFIGURATION STRAPS

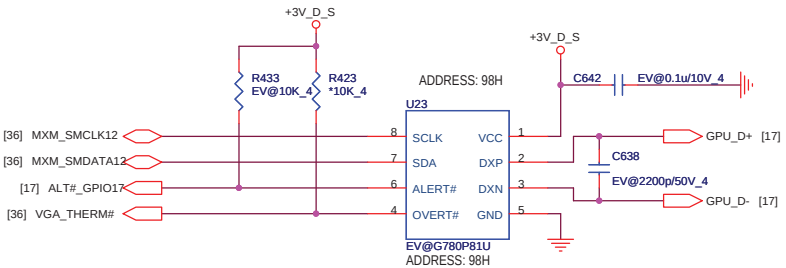
**ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET**

| STRAPS | PIN | DESCRIPTION OF DEFAULT SETTINGS | DEFAULT | REMARK |
|---|---|---|---|---|
| TX_PWRS_ENB | GPIO0 | 0 = 50% TX OUTPUT SWING<br>1 = FULL TX OUTPUT SWING | 0 | |
| TX_DEEMPH_EN | GPIO1 | PCIE TRANSMITTER DE-EMPHASIS ENABLED<br>0 = TX DE-EMPHASIS DISABLED<br>1 = TX DE-EMPHASIS ENABLED | 0 | |
| BIOS_ROM_EN | GPIO_22_ROMCSB | Enable external BIOS ROM device<br>0 - Disable external BIOS ROM device<br>1 - Enable external BIOS ROM device | 0 | |
| ROMIDCFG[2:0] | GPIO[13:11] | SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT | 001 | See ROM table |
| BIF_GEN2_EN_A | GPIO2 | 0 = PCIE DEVICE AS 2.5GT/S CAPABLE<br>1 = PCIE DEVICE AS 5GT/S CAPABLE | 0 | |
| GPIO_8_ROMSO<br>H2SYNC<br>GPIO_21_BB_EN | GPIO8<br>H2SYNC<br>GPIO21 | Reserved Only | 0 | |
| AUD[1]<br>AUD[0] | HSYNC<br>VSYNC | AUD[1:0]<br>00: NO AUDIO FUNCTION.<br>01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED.<br>10: AUDIO FOR DISPLAYPORT ONLY.<br>11: AUDIO FOR BOTH DISPLAYPORT AND HDMI. | 11 | See Audio table |
| GPIO_9_ROMSI | GPIO9 | 0 = VGA controller capacity enable | 0 | |
| VIP_DEVICE_STRAP_ENA | V2SYNC | 0 = DRIVER would ignore the value sample on VHAD_0 during RESET. | 0 | |

## Thermal Sensor(VGA)

| Vendor | P/N |
|---|---|
| WINDBOND | AL83L771K01 |
| GMT | AL000780000 |

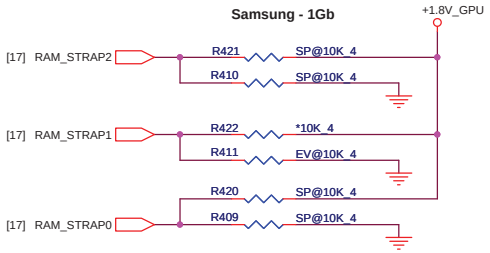
USD0.16




## DDR3 Memory Aperture size(GPU)

### DDR3 Memory size

| Vendor | Vendor P/N | STN B/S P/N | RAM_STRAP2<br>DVPDATA_2 | RAM_STRAP1<br>DVPDATA_1 | RAM_STRAP0<br>DVPDATA_0 |
|---|---|---|---|---|---|
| Hynix | | | 1 | 1 | 0 |
| | H5TQ1G63BFR-12C | AKD5LZGTW04 (64M*16) | 1 | 0 | 0 |
| | H5TQ2G63BFR-12C | AKD5MGGTW03 (128M*16) | 1 | 0 | 1 |
| Samsung | | | | | |
| | K4W1G1646E-HC12 | AKD5LGGT506 (64M*16) | 0 | 0 | 0 |
| | K4W2G1646B-HC12 | AKD5MGGT500 (128m*16) | 0 | 0 | 1 |
| AMD | 23EY2387MA12-SZ | AKD5LGGT700 | 0 | 1 | 0 |
| | | | | | |




RAM_STRAP2 SET DDR3 Vendor
RAM_STRAP[1:0] SET SIZE.

Quanta Computer Inc.
PROJECT : ZRD

| Size | Document Number | Rev |
|---|---|---|
| | Strip/Thermal | 1C |
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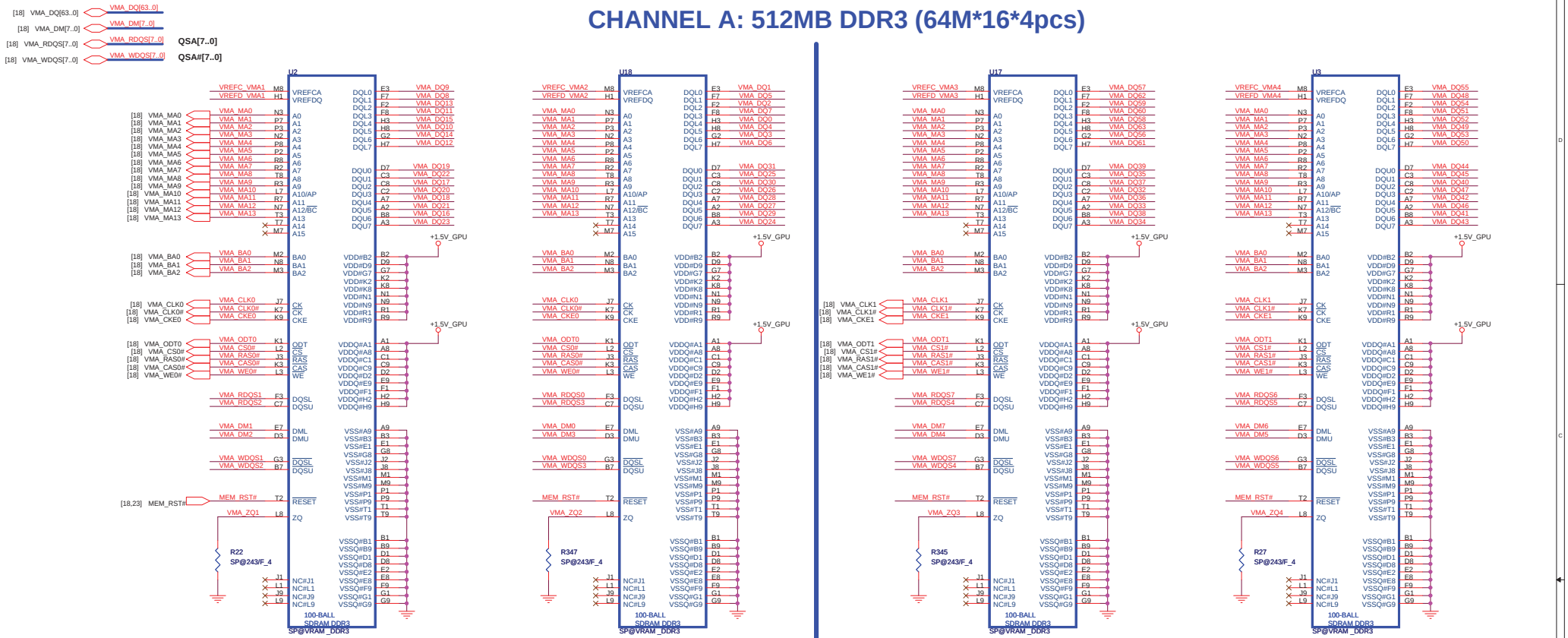
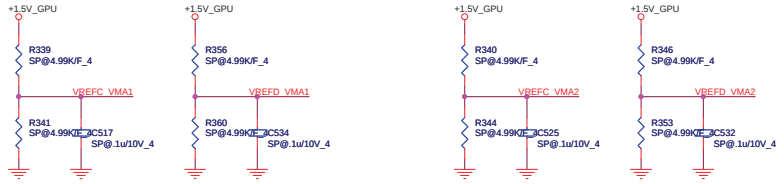
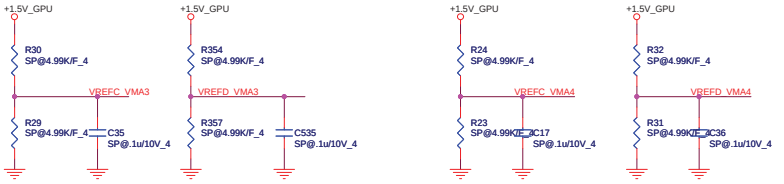
# CHANNEL A: 512MB DDR3 (64M*16*4pcs)



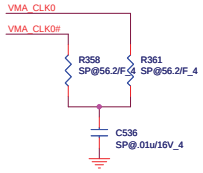

## Group-A0 VREF



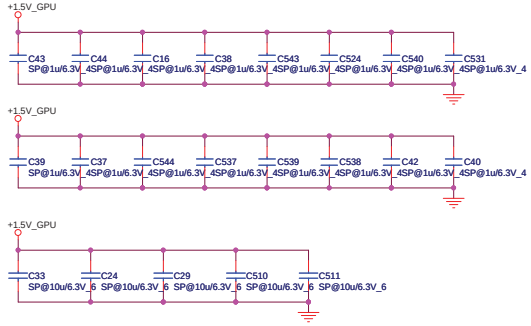

## Group-A1 VREF



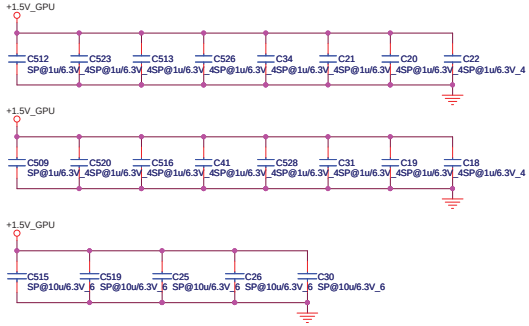

## MEM_A0 CLK



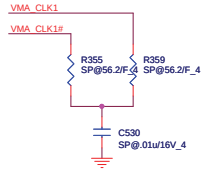

## Group-A0 decoupling CAP




## Group-A1 decoupling CAP




## MEM_A1 CLK




Quanta Computer Inc.

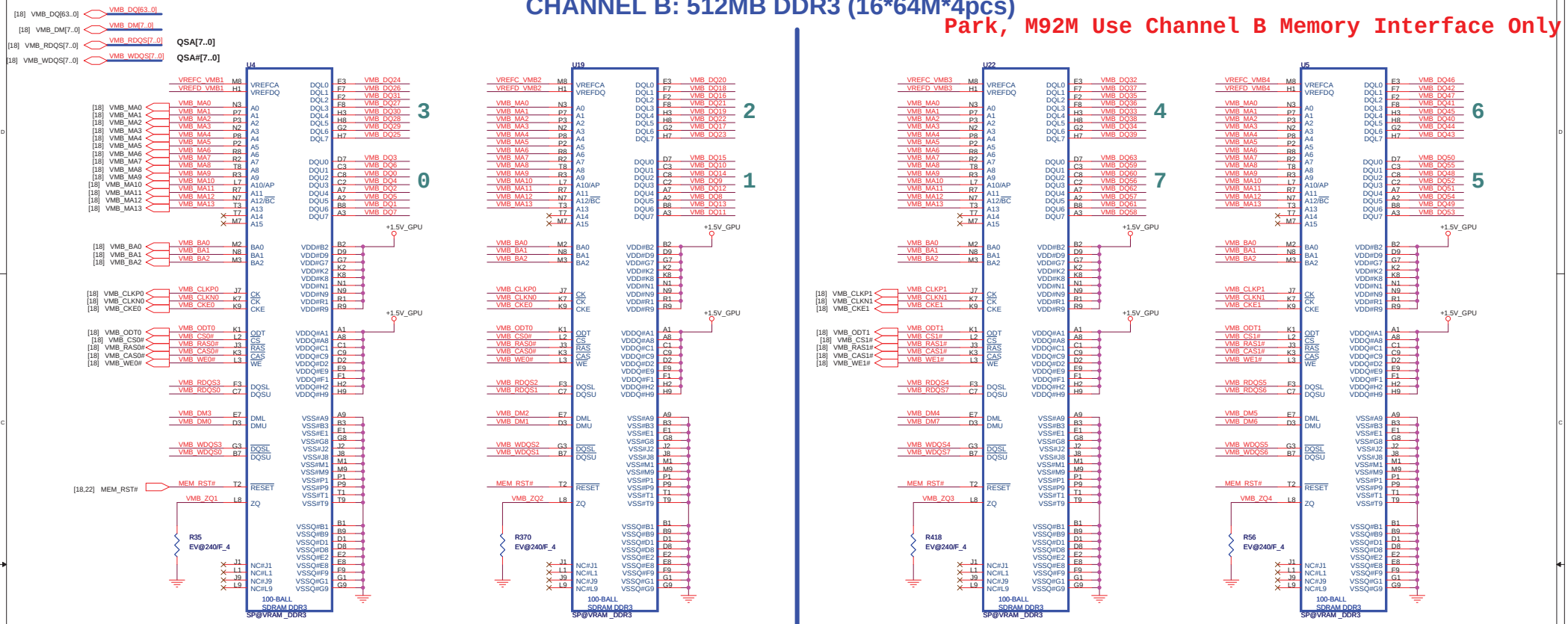
PROJECT : ZRD

| Size | Document Number | Rev |
|---|---|---|
| | MEMORY 1 channel A | 1C |

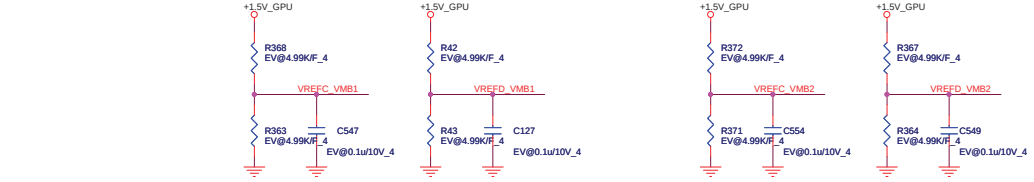
Date: Wednesday, July 21, 2010 Sheet 22 of 46

# CHANNEL B: 512MB DDR3 (16*64M*4pcs)

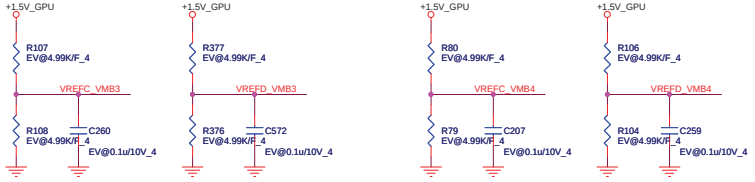
**Park, M92M Use Channel B Memory Interface Only**



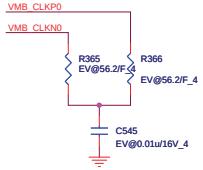

## Group-B0 VREF



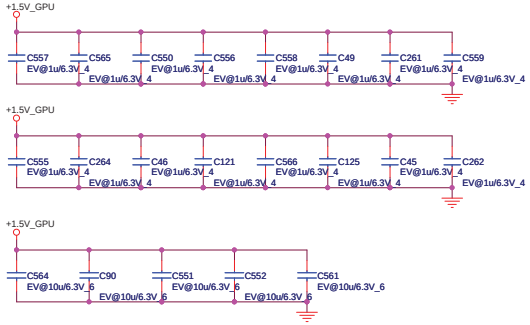

## Group-B1 VREF



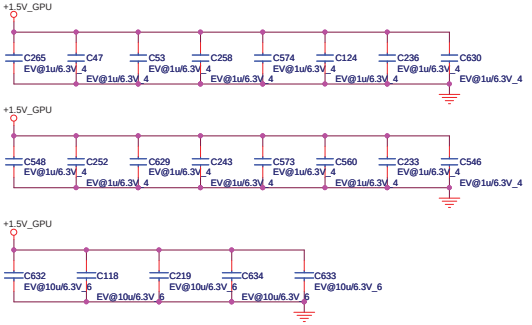

## MEM_B0 CLK



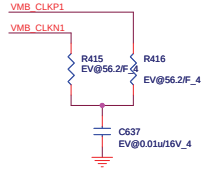

## Group-B0 decoupling CAP




## Group-B1 decoupling CAP



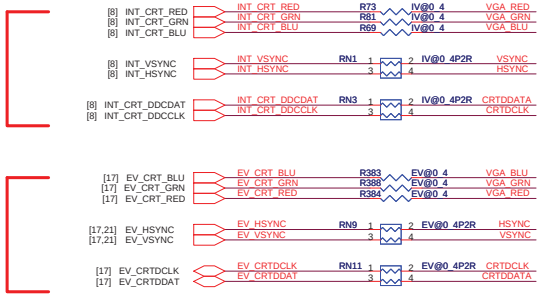

## MEM_B1 CLK



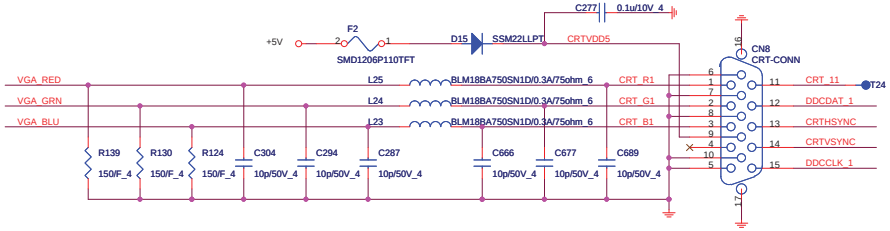

| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT : ZRD | | |
| Size | Document Number: MEMORY 2 channel B | Rev: 1C |
| Date: Wednesday, July 21, 2010 | Sheet 23 of 46 | |

## CRT Switch

0_ohm Resistor place close to Joint-Point

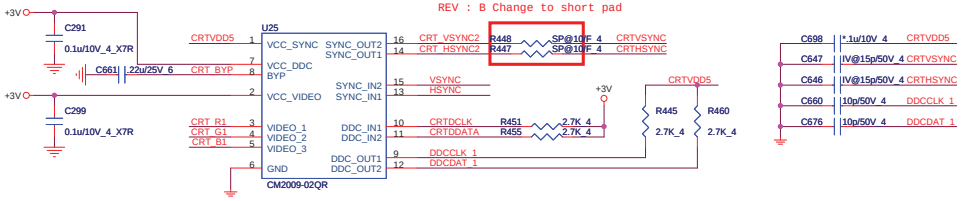



## CRT



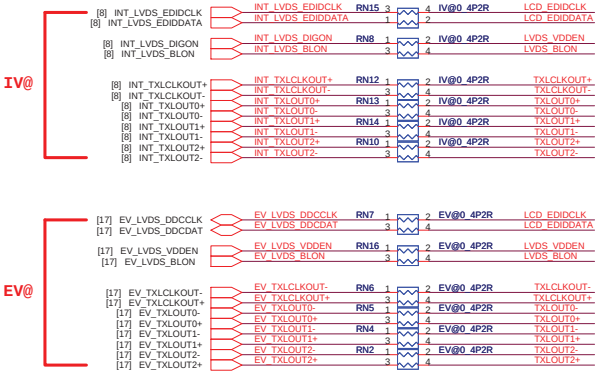

REV : C Change to 0402 R

REV : B Change to short pad



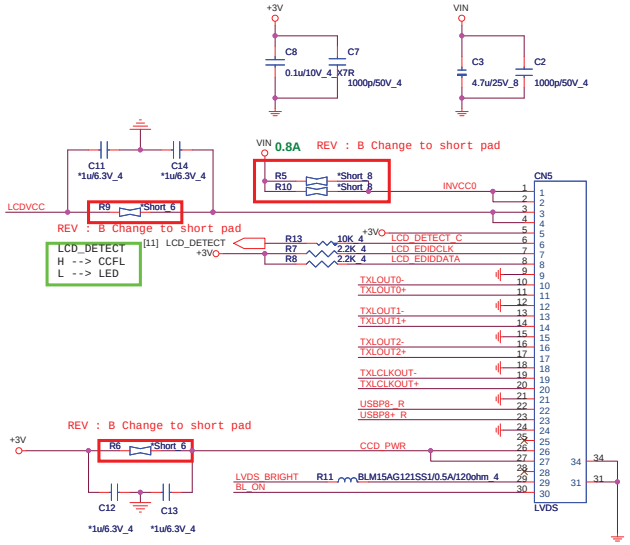

## LVDS

0_ohm Resistor place close to Joint-Point

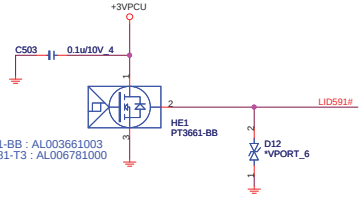



CCD +3V-current budget 0.2A

## LVDS

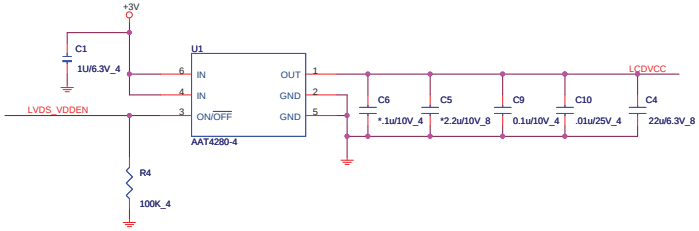



## Lid Switch (Hall sensor)

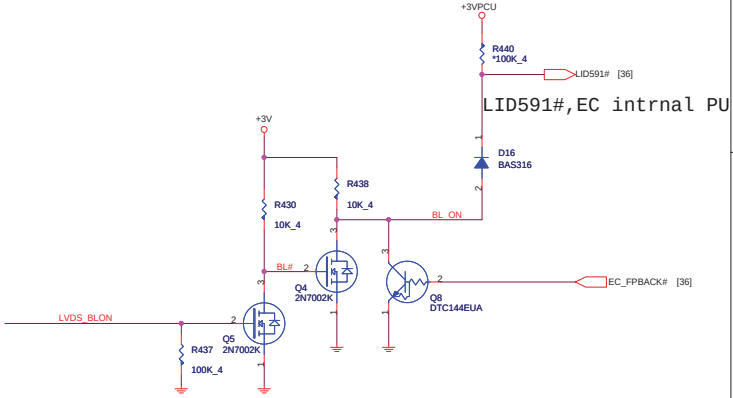



PT3661-BB : AL003661003
EM-6781-T3 : AL006781000

## LCD Power



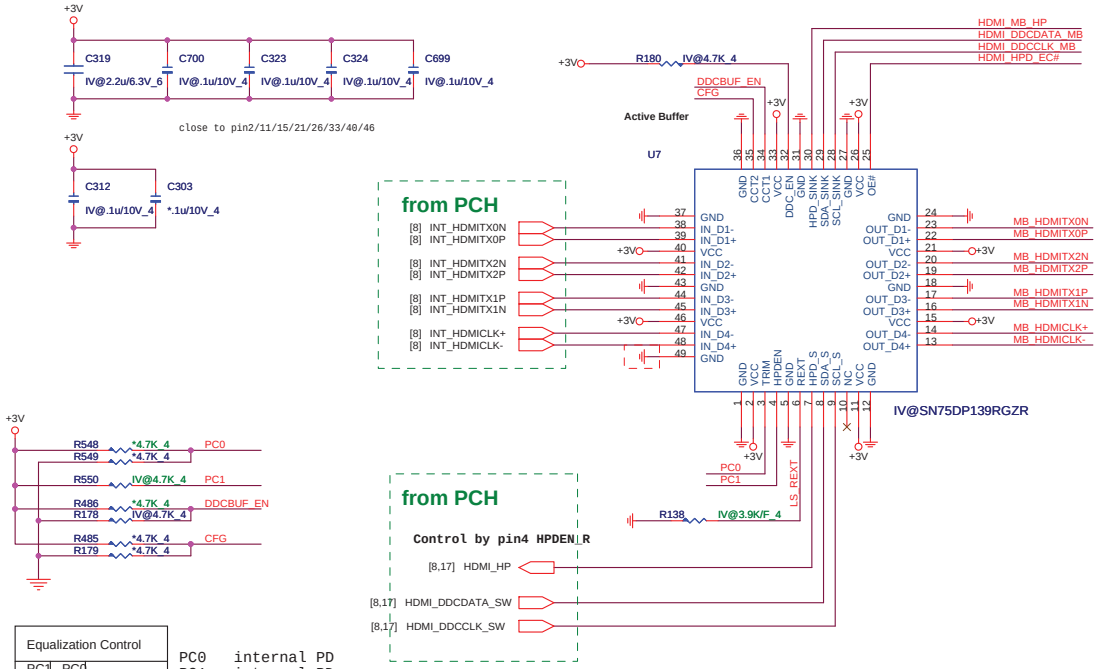

## Backlight Control




| | | | |
|---|---|---|---|
| Quanta Computer Inc. PROJECT : ZRD | | | |
| Size | Document Number | CRT/LVDS/CAMERA/LID | Rev 1C |
| Date: Wednesday, July 21, 2010 | | Sheet 24 of 46 | |

## HDMI LEVEL SHIFTER

IV@

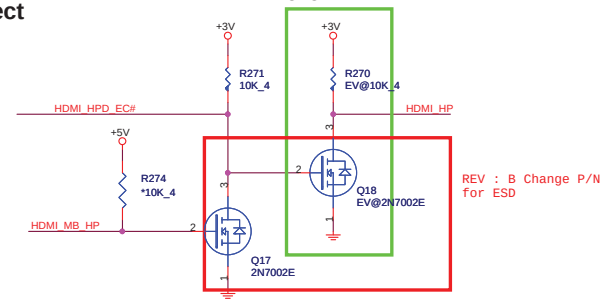



| Equalization Control | | |
|---|---|---|
| PC1 PIN4 | PC0 PIN3 | EQ Control |
| L | L | 8dB |
| L | H | 4dB |
| H | L | 12dB |
| H | H | 0dB |

PC0 internal PD
PC1 internal PD
DDCBUF_EN internal PD
CFG internal PD
DDC_EN internal PU

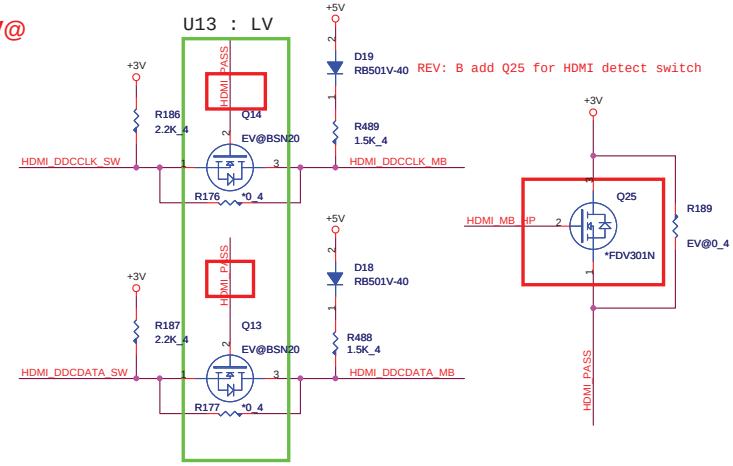
## HDMI-detect

EV@



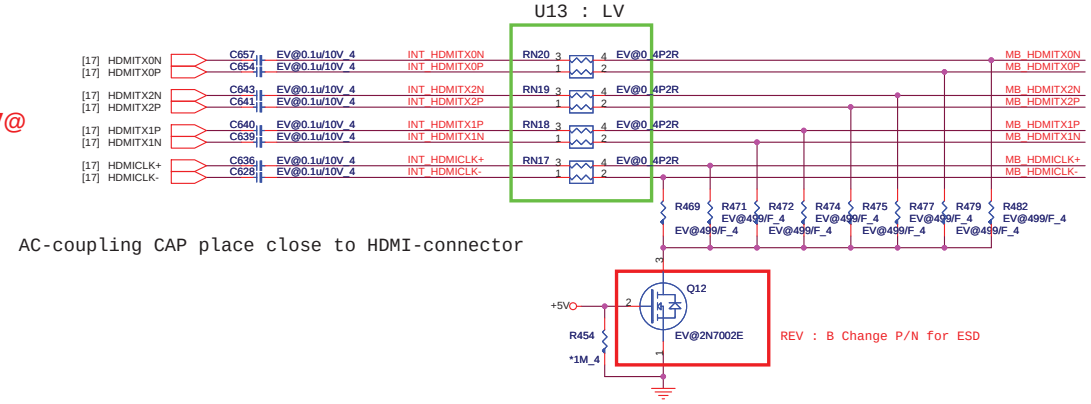

## I2C

EV@



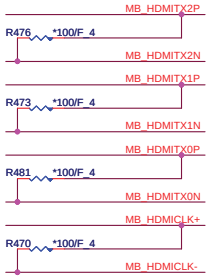

## Switchable Graphic HDMI source

EV@




AC-coupling CAP place close to HDMI-connector

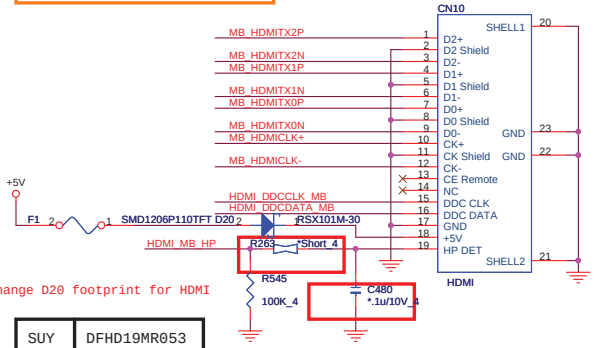
## EMI




REV C: Change D20 footprint for HDMI

## HDMI connector

REV : C Location :D20 Change Footprint & P/N

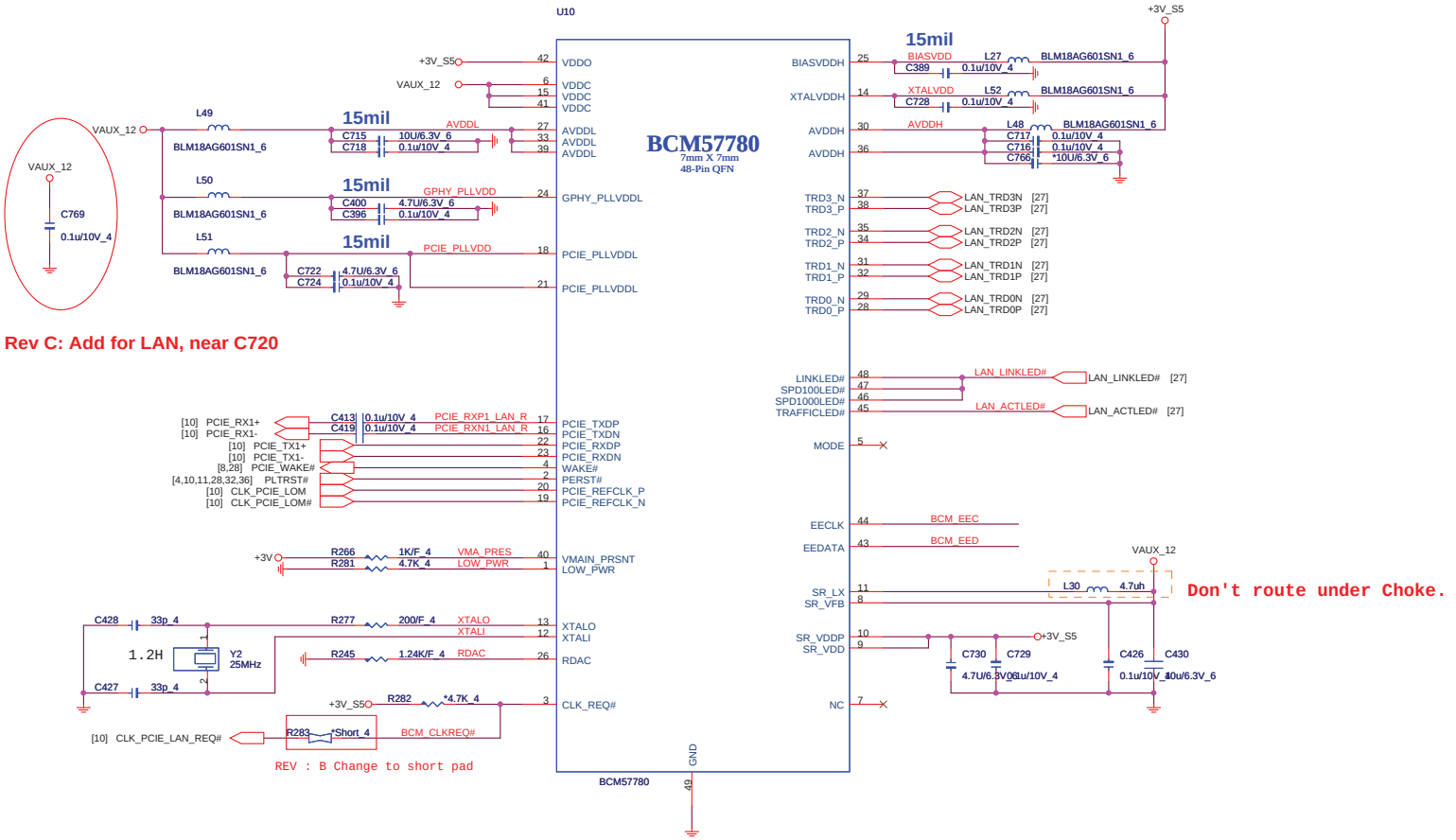



| | |
|---|---|
| SUY | DFHD19MR053 |
| LTS | DFHD19MR085 |

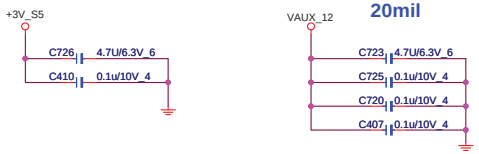
Quanta Computer Inc.
PROJECT : ZRD

| Size | Document Number | Rev |
|---|---|---|
| | HDMI (PS8101) | 1C |
| Date: Wednesday, July 21, 2010 | Sheet 25 of 46 | |

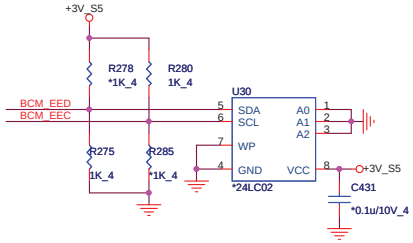
# Giga-LAN BCM57780




## LAN POWER




## EEPROM




**EEPROM Strapping**

| EEPROM Type | EECLK | EEDATA |
|---|---|---|
| 24LC02 | 1 | 1 |
| Internal | 1 | 0 |

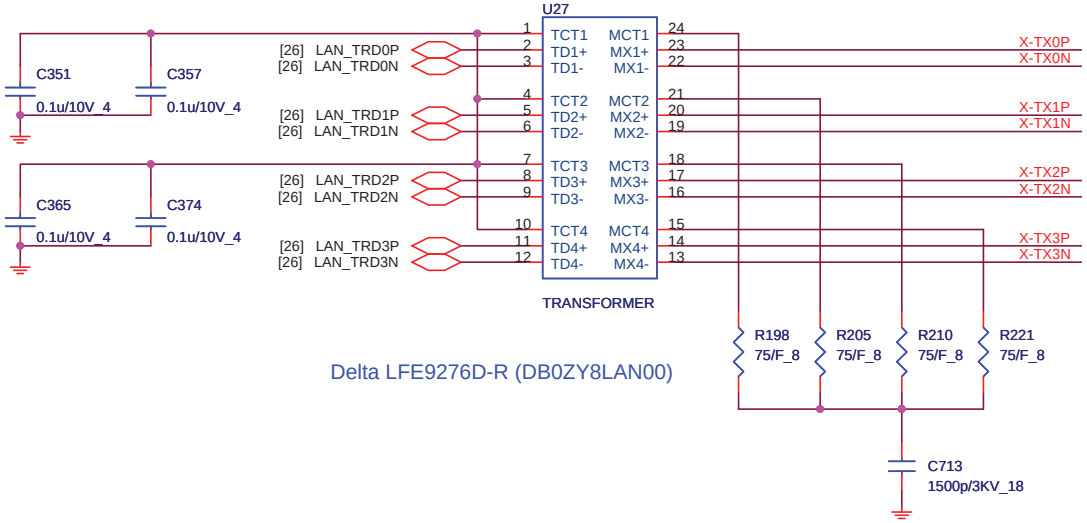
Quanta Computer Inc.
PROJECT : ZRD

| Size | Document Number | Rev |
|---|---|---|
| | GLAN BCM57780 | 1C |

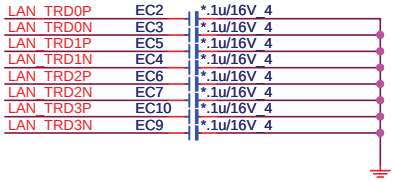
Date: Wednesday, July 21, 2010 Sheet 26 of 46

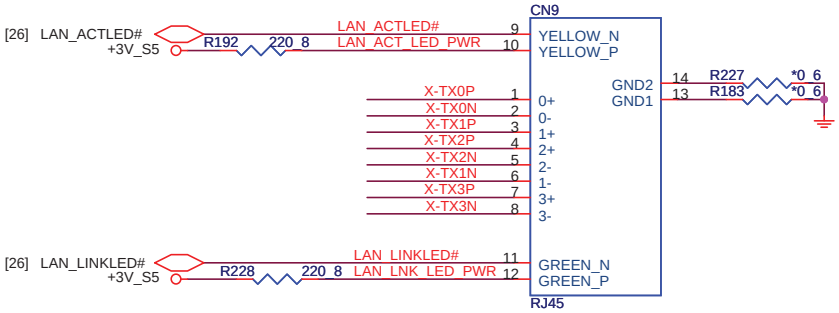
# TRANSFORMER

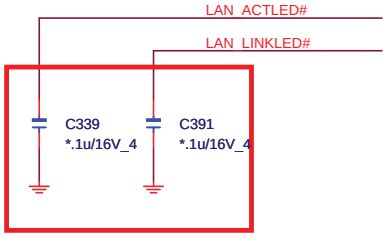
| | |
|---|---|
| SUY | DFTJ12FR109 |
| AEC | DFTJ12FR135 |




Delta LFE9276D-R (DB0ZY8LAN00)




REV : B Change to 0402 for ESD

**Quanta Computer Inc.**

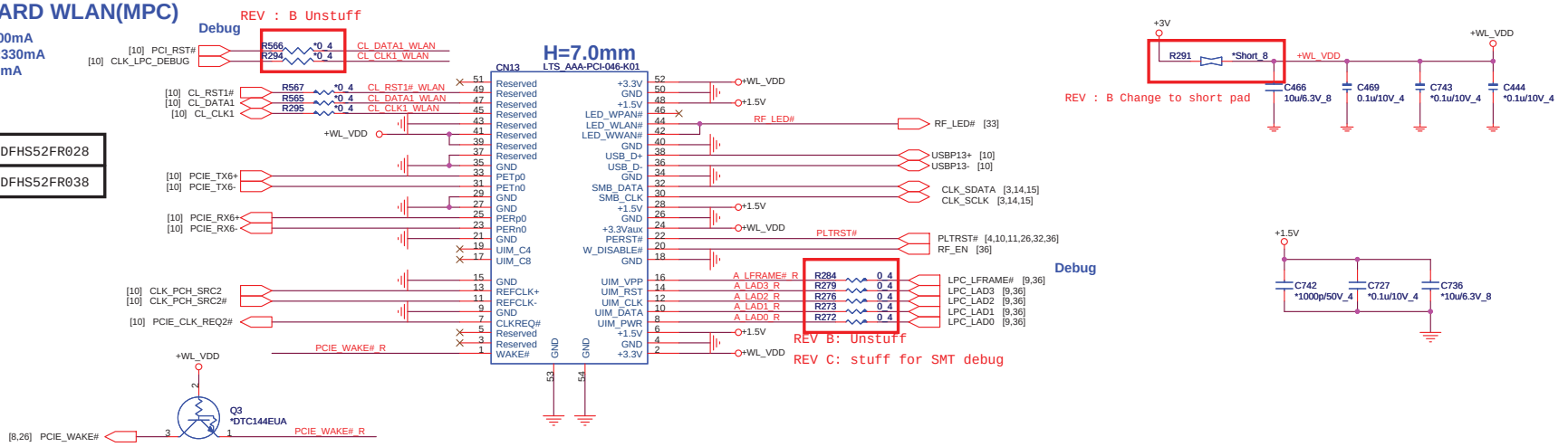
**PROJECT : ZRD**

| Size | Document Number | Rev |
|---|---|---|
| | LAN Transformer and RJ45 | 1C |
| Date: Wednesday, July 21, 2010 | Sheet 27 of 46 | |

# MINI-CARD WLAN(MPC)

+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

| | |
|---|---|
| PTI | DFHS52FR028 |
| LTS | DFHS52FR038 |







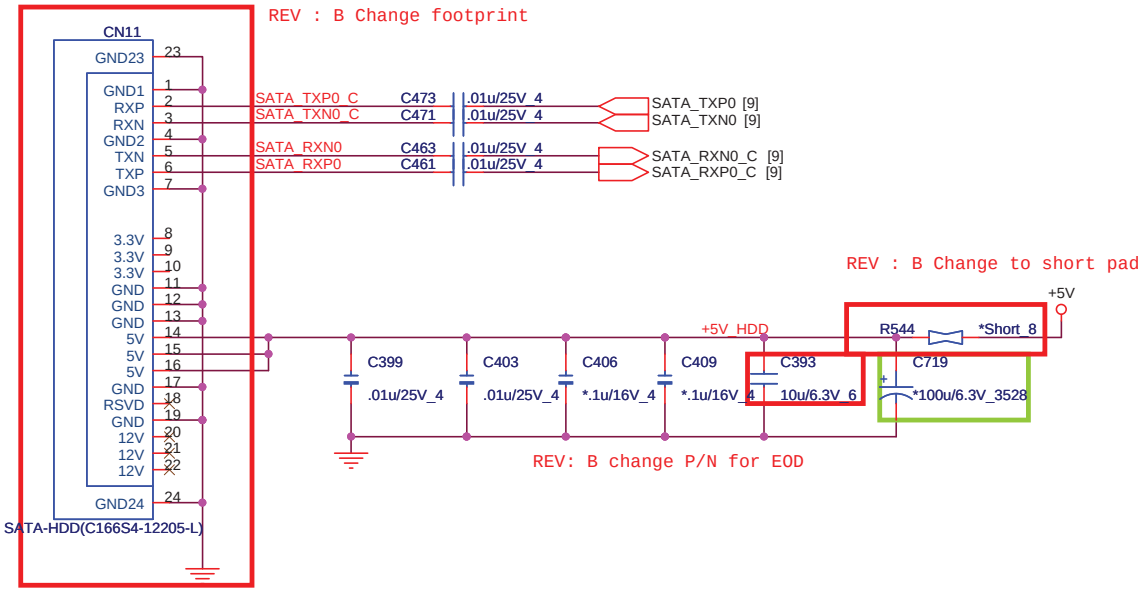



Quanta Computer Inc.
PROJECT : ZRD

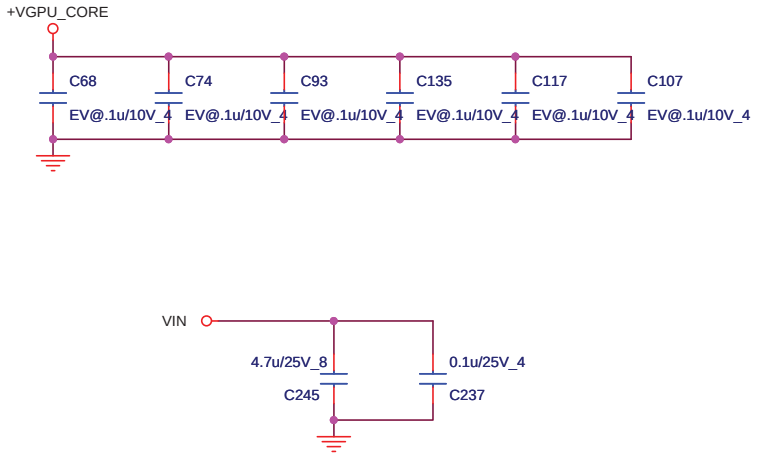
| Size | Document Number | Rev |
|---|---|---|
| | MINI PCI-E card/TV | 1C |

Date: Wednesday, July 21, 2010 Sheet 28 of 46

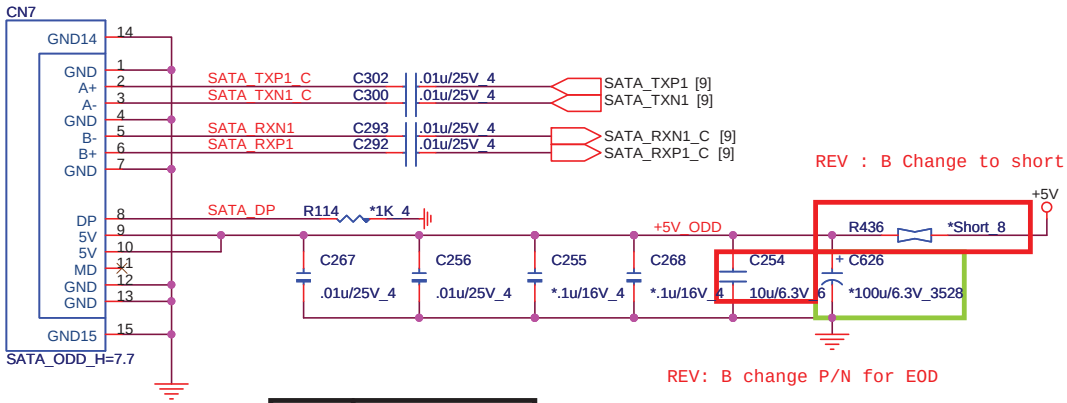
## MAIN SATA HDD




## EE RETURN-PATH CAPACITORS




## ODD (SATA)




| | |
|---|---|
| SUY | DFHS22FR214 |
| AOP | DFHS22FR232 |
| AEC | DFHS22FR216 |

| | |
|---|---|
| AOP | DFHS13FR011 |
| OTK | DFHS13FR010 |

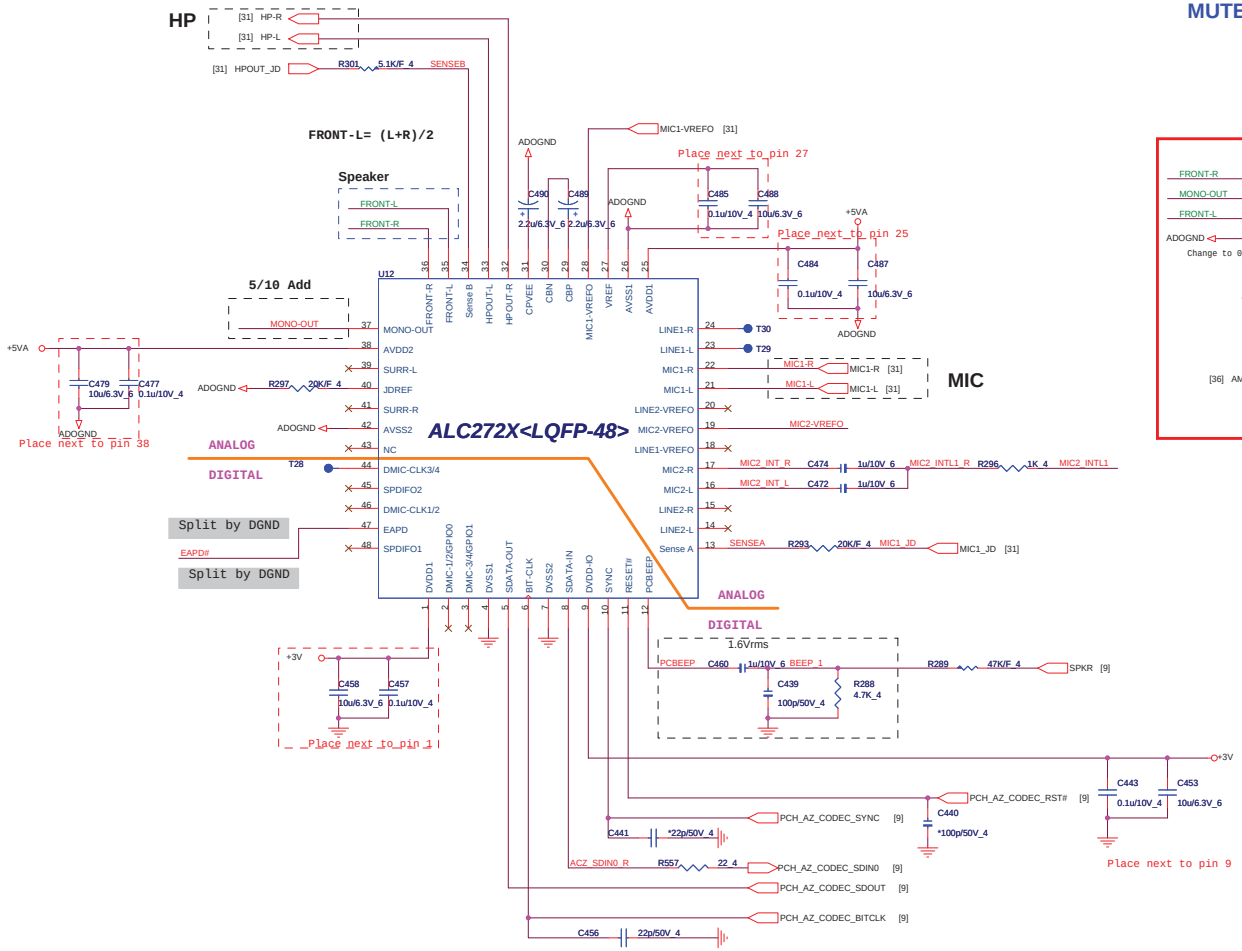
Quanta Computer Inc.

PROJECT : ZRD

| Size | Document Number | Rev |
|---|---|---|
| | SATA-HDD/ODD/RETURN-PATH | 1C |

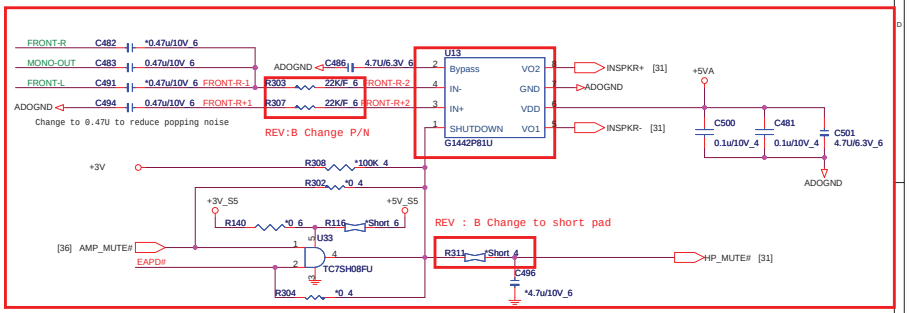
Date: Wednesday, July 21, 2010 Sheet 29 of 46

## Codec(ADO)

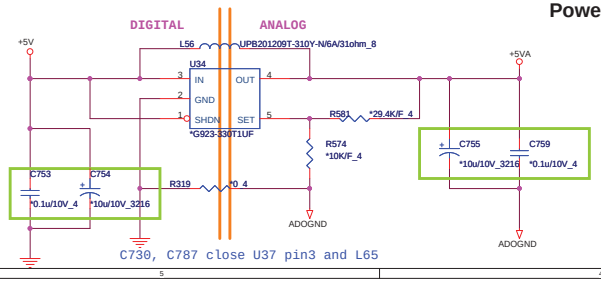



## MUTE(AMP)

REV : B Change AMP circuit

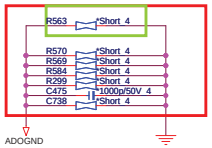



## Power (ADO)



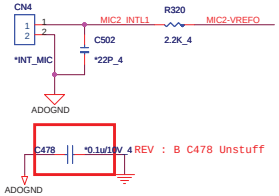

REV : B C478 Change to short pad and
Stuff R563 ,R570 ,R569 ,R584 ,R299 ,C738

Place in Bottom of codec




**Tied at one point only under the codec or near the codec**

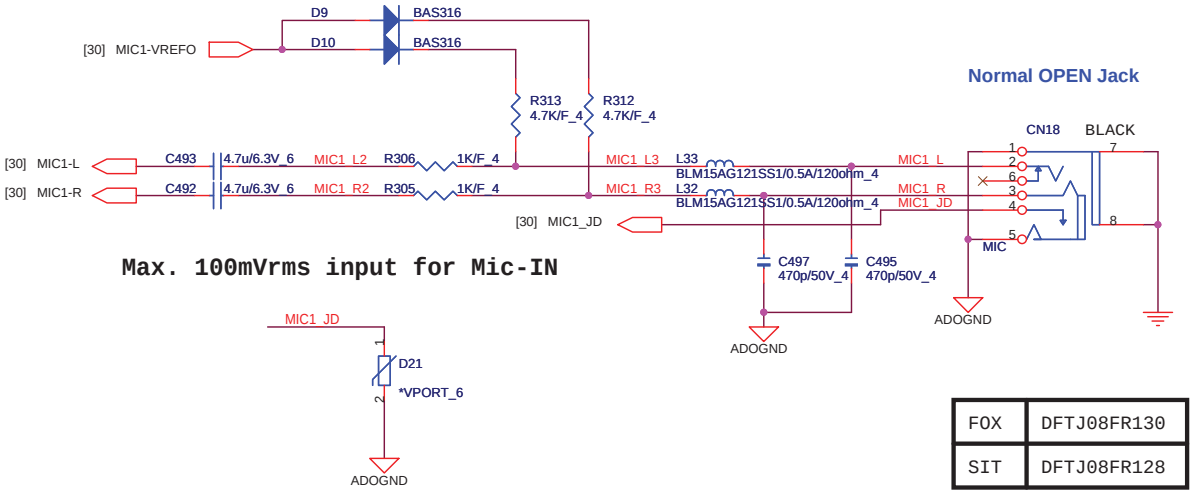
## INT MIC array




cap place close to MIC-connector

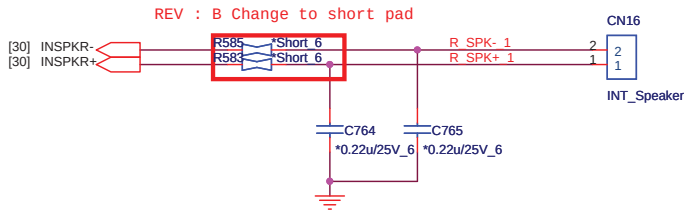
| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT : ZRD | | |
| Size | Document Number: REALTEK ALC663&888/MDC | Rev: 1C |
| Date: Wednesday, July 21, 2010 | Sheet 30 of 46 | |

## MIC



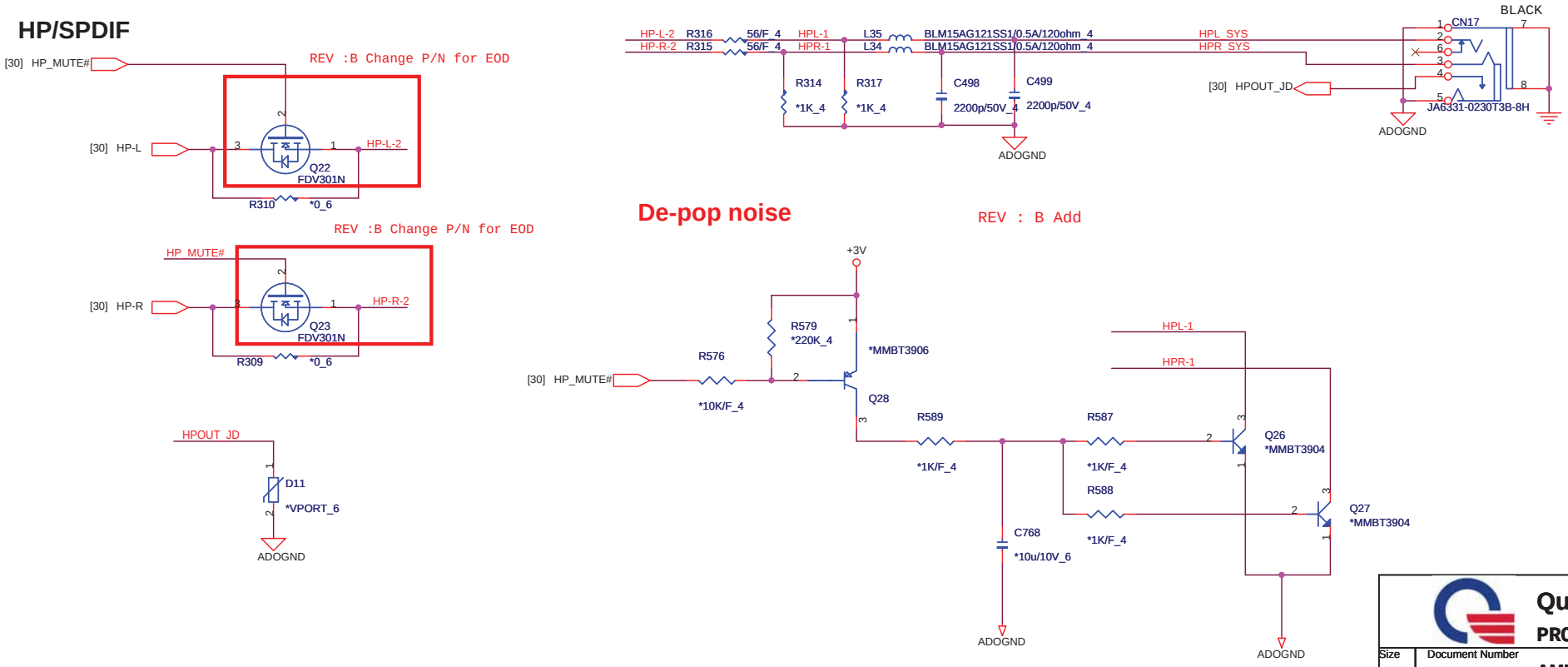

| | |
|---|---|
| FOX | DFTJ08FR130 |
| SIT | DFTJ08FR128 |

## Internal Speaker




| | |
|---|---|
| ACS | DFHD02MR311 |
| PTI | DFHD02MR508 |

## HP/SPDIF




Quanta Computer Inc.

PROJECT : ZRD

| Size | Document Number | Rev |
|---|---|---|
| | AMP /AUDIO JACK CONN | 1C |

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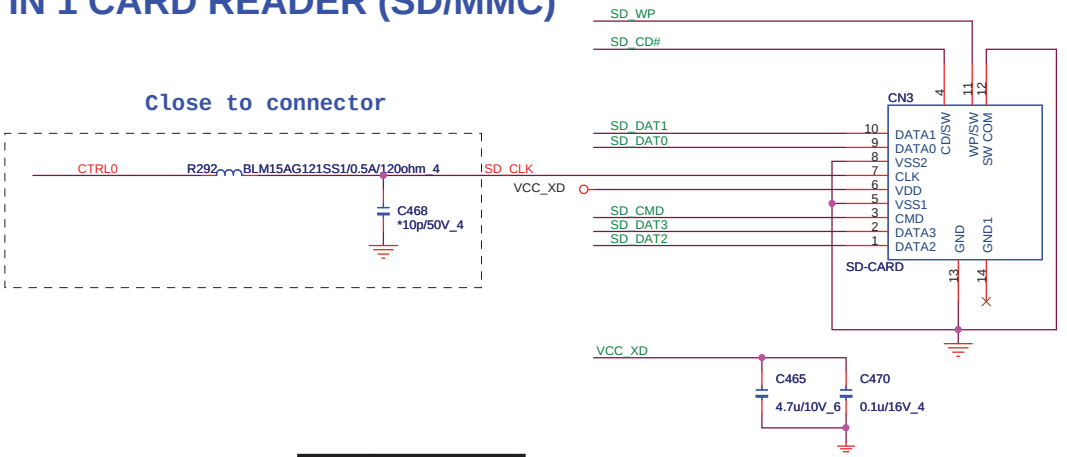
# CARD READER Controller

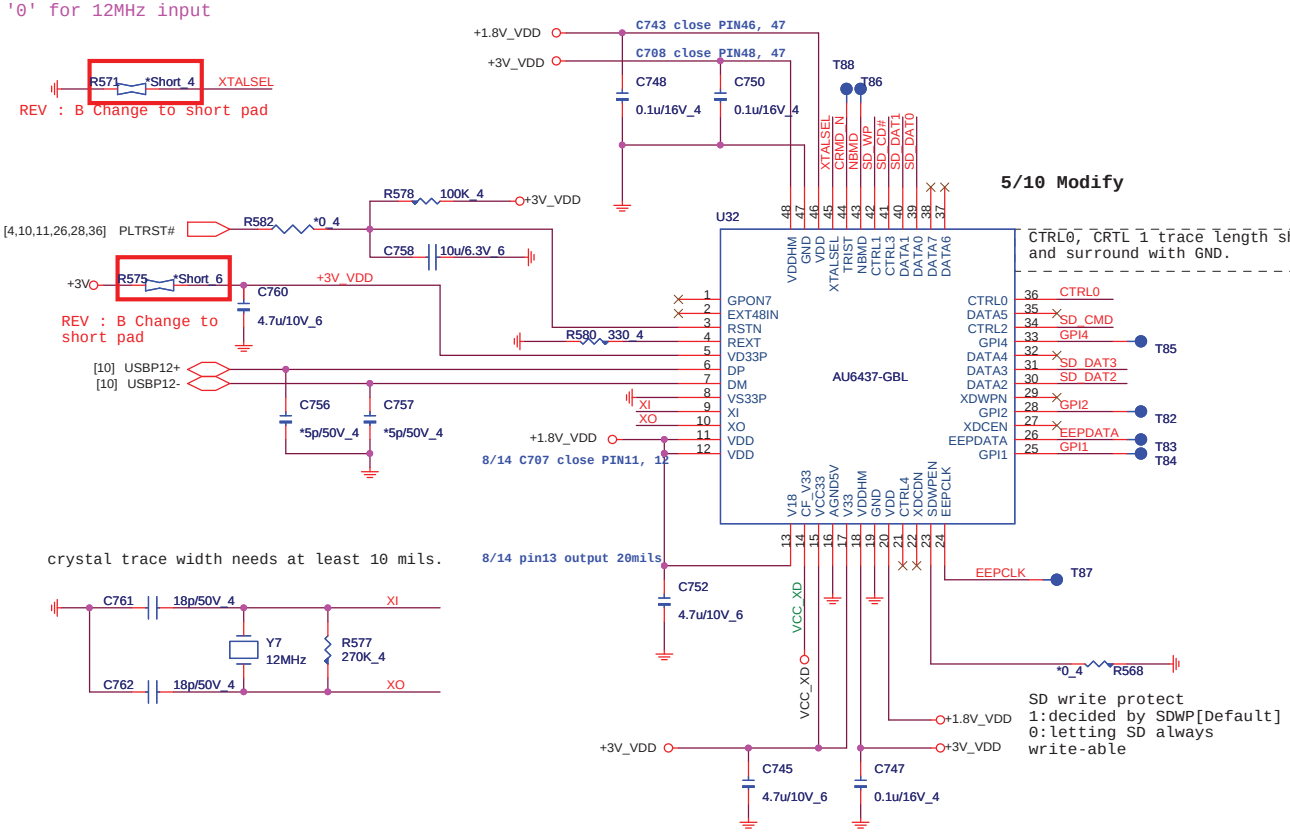
# 2 IN 1 CARD READER (SD/MMC)




Close to CN14 pin 14 & pin23
4.7u CAP close to pin23

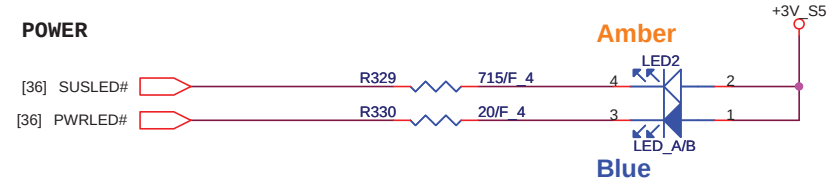
| | |
|---|---|
| PNT | DFHS11FR011 |
| PLA | DFHS11FR033 |

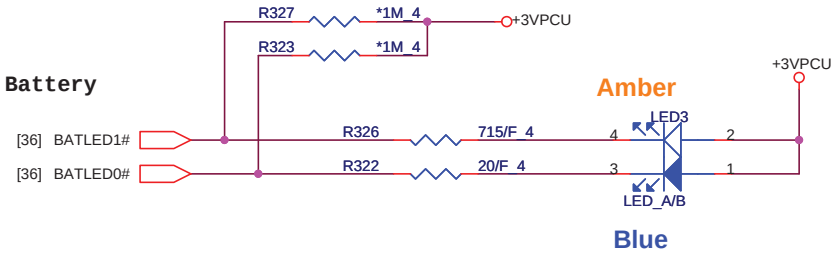
Clock input selection
'1' for 48MHz input [Default,Internal PU]
'0' for 12MHz input

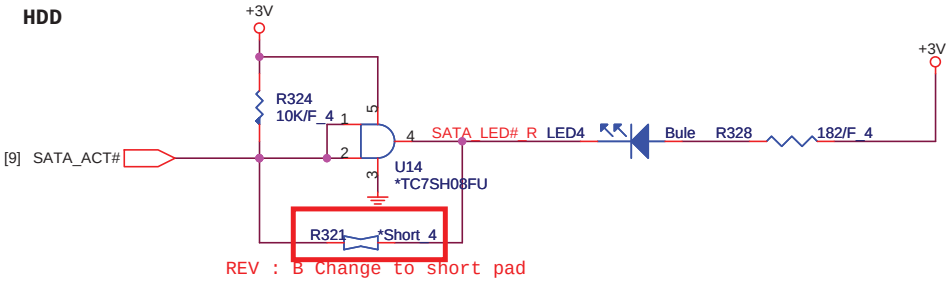


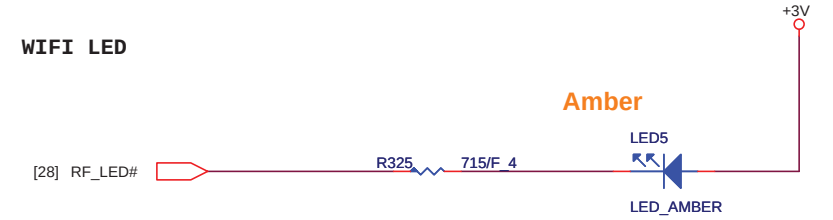

| | | | |
|---|---|---|---|
| PROJECT : ZQ5 Quanta Computer Inc. | | | |
| Size | Document Number AU6433 CardReader | | Rev 1C |
| Date: | Wednesday, July 21, 2010 | Sheet 32 of 43 | |

# LED



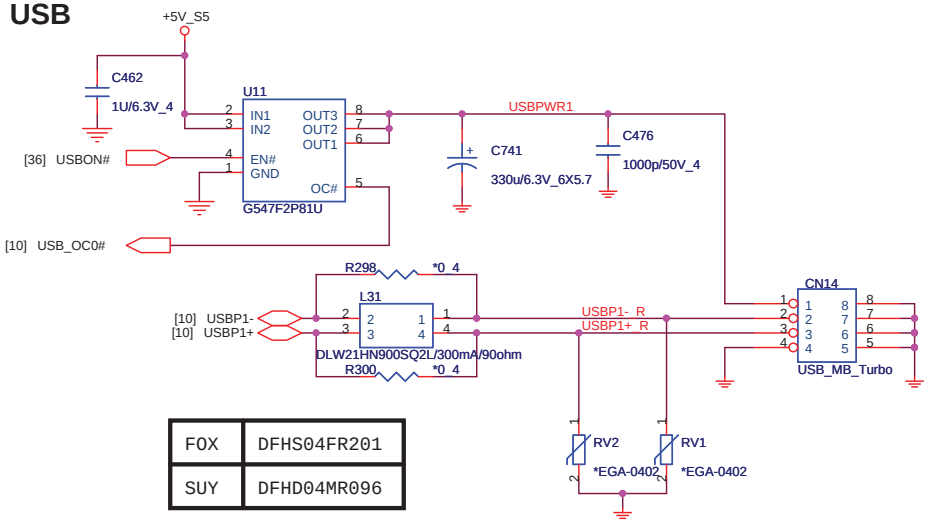



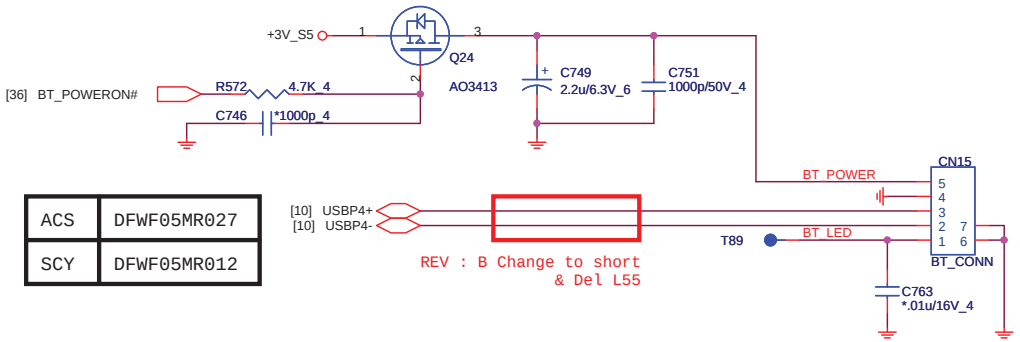

| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT : ZRD | | |
| Size | Document Number: POWER/MMB/LAUNCH/LED | Rev: 1C |
| Date: Wednesday, July 21, 2010 | Sheet 33 of 46 | |

## USB



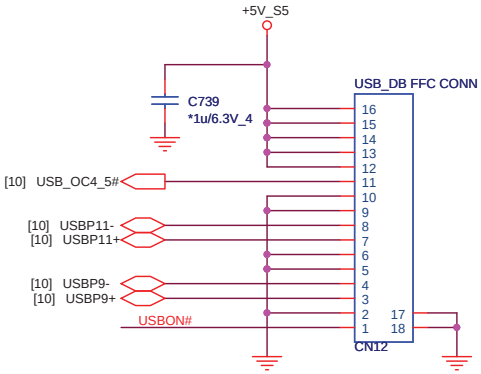

| | |
|---|---|
| FOX | DFHS04FR201 |
| SUY | DFHD04MR096 |

## BLUETOOTH CONNECTOR




| | |
|---|---|
| ACS | DFWF05MR027 |
| SCY | DFWF05MR012 |

## USB/B




Quanta Computer Inc.

PROJECT : ZRD

| Size | Document Number | Rev |
|---|---|---|
| | USB/ BT | 1C |

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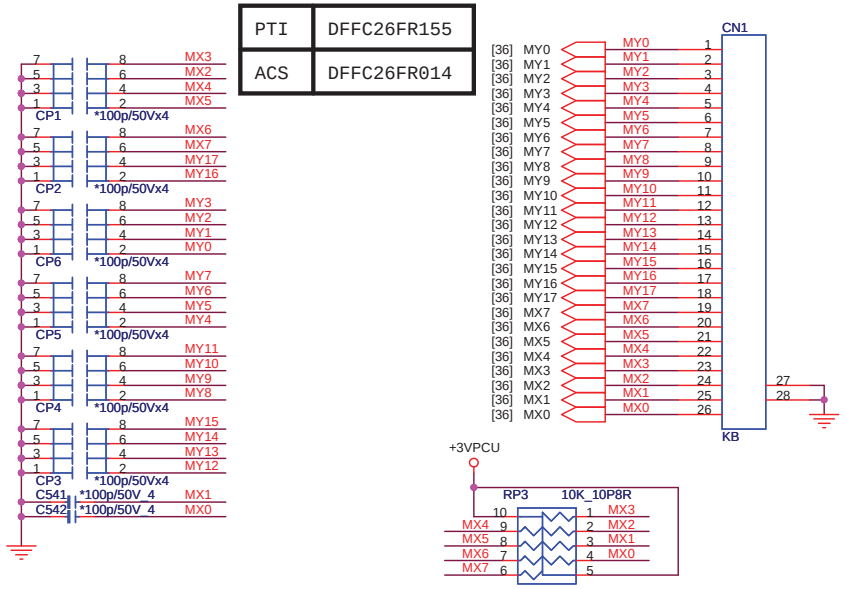
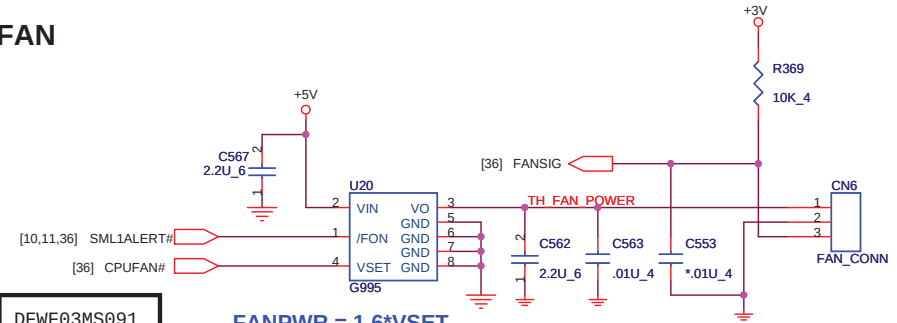
## K/B

| | |
|---|---|
| PTI | DFFC26FR155 |
| ACS | DFFC26FR014 |



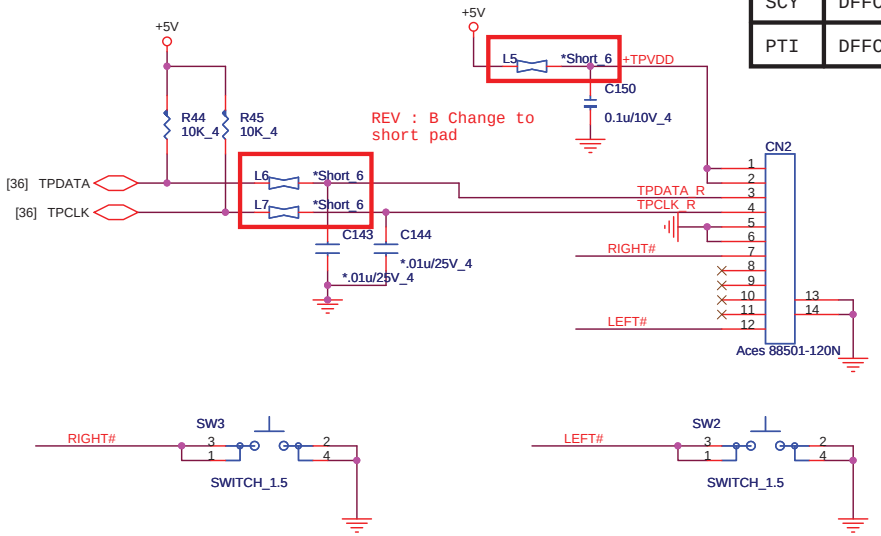

## CPU FAN

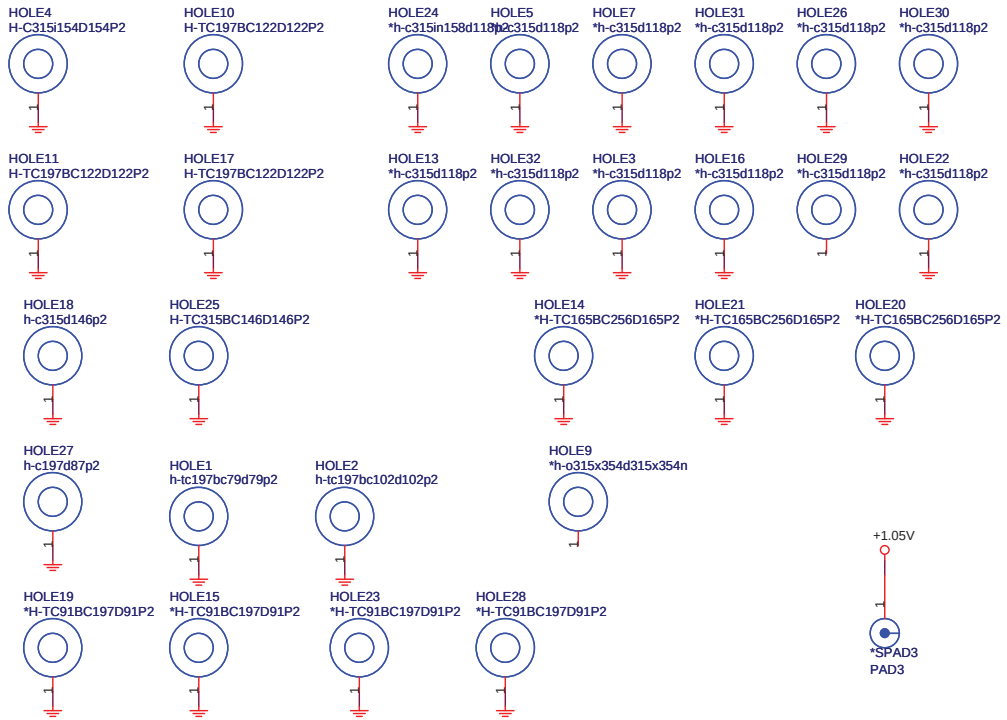
| | |
|---|---|
| ACS | DFWF03MS091 |
| SCY | DFWF03MS000 |

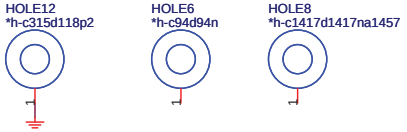



## TOUCHPAD & Switch CONN.

| | |
|---|---|
| ACS | DFFC12FR017 |
| SCY | DFFC12FR015 |
| PTI | DFFC12FR234 |




Quanta Computer Inc.

PROJECT : ZRD

| Size | Document Number | Rev |
|---|---|---|
| | KB/FAN/TP+FP | 1C |

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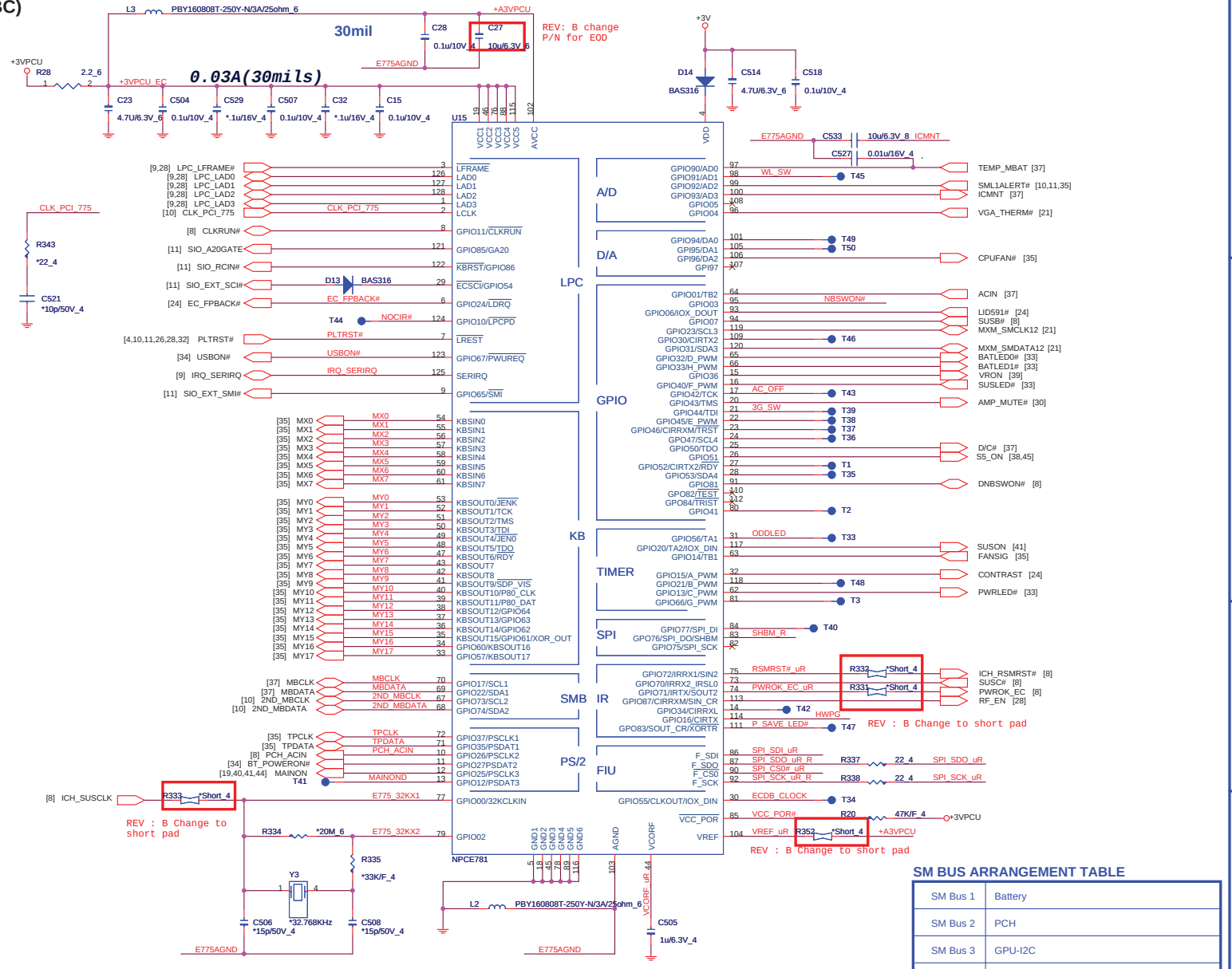
## EC(KBC)




## SM BUS ARRANGEMENT TABLE

| | |
|---|---|
| SM Bus 1 | Battery |
| SM Bus 2 | PCH |
| SM Bus 3 | GPU-I2C |
| SM Bus 4 | N/A |

## I/O ADDRESS SETTING(KBC)

SHBM=0: Enable shared memory with host BIOS

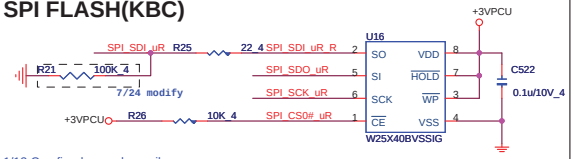
SHBM R336 *10K_4

1/13 Comfirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

## SM BUS PU(KBC)

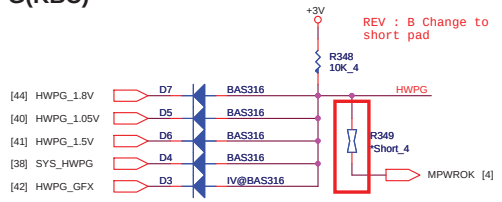
+3VPCU
MBCLK R19 10K_4
MBDATA R18 10K_4
+3V_D_S
MXM_SMCLK12 R350 EV@2.2K_4
MXM_SMDATA12 R351 EV@2.2K_4
+3V
2ND_MBCLK R16 10K_4
2ND_MBDATA R17 10K_4
VGA_THERM# R342 EV@10K_4

## SPI FLASH(KBC)

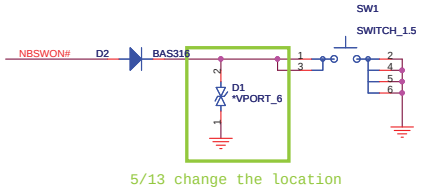



1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

## HWPG(KBC)




## POWER-ON Switch(KBC)

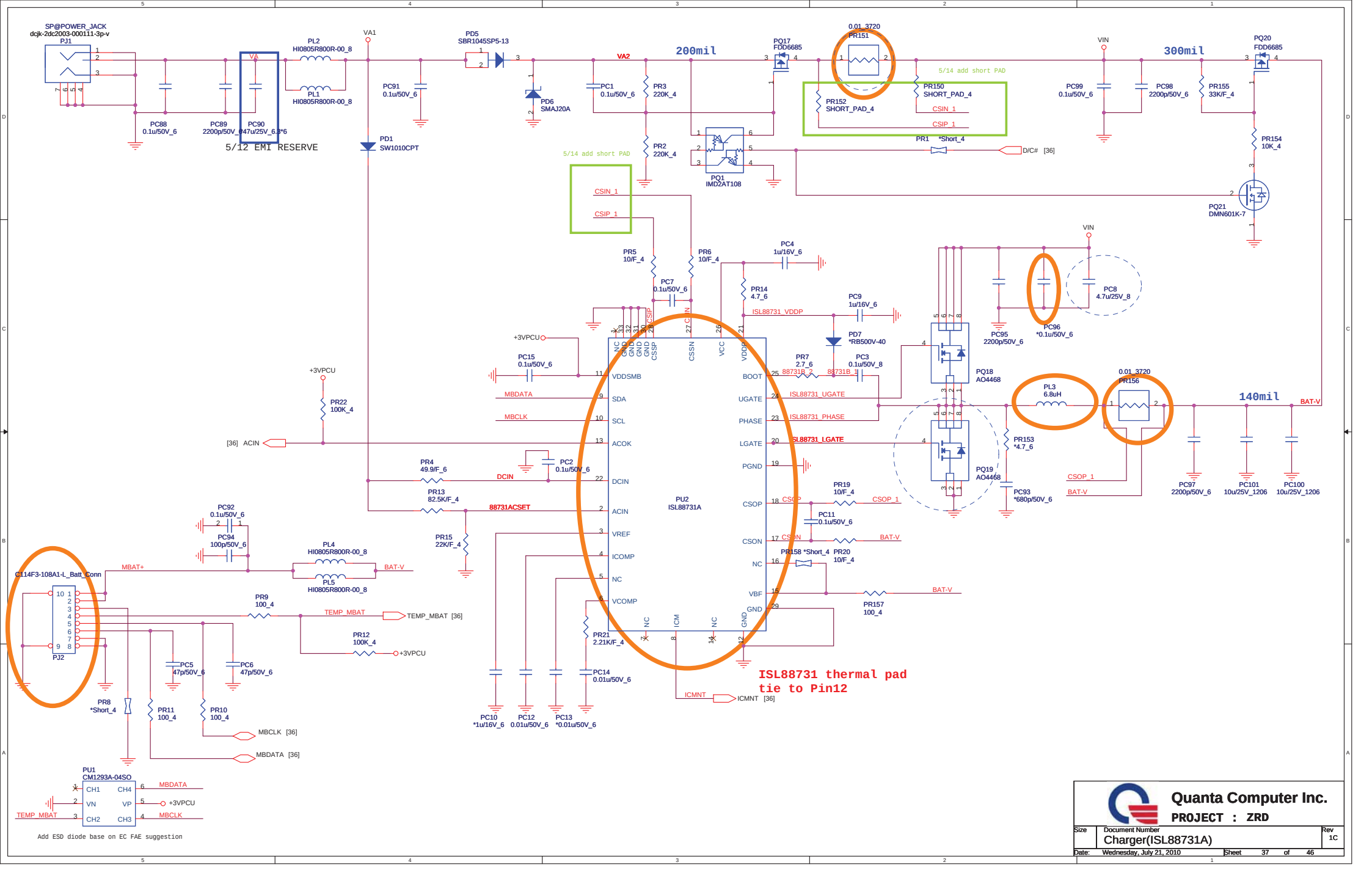


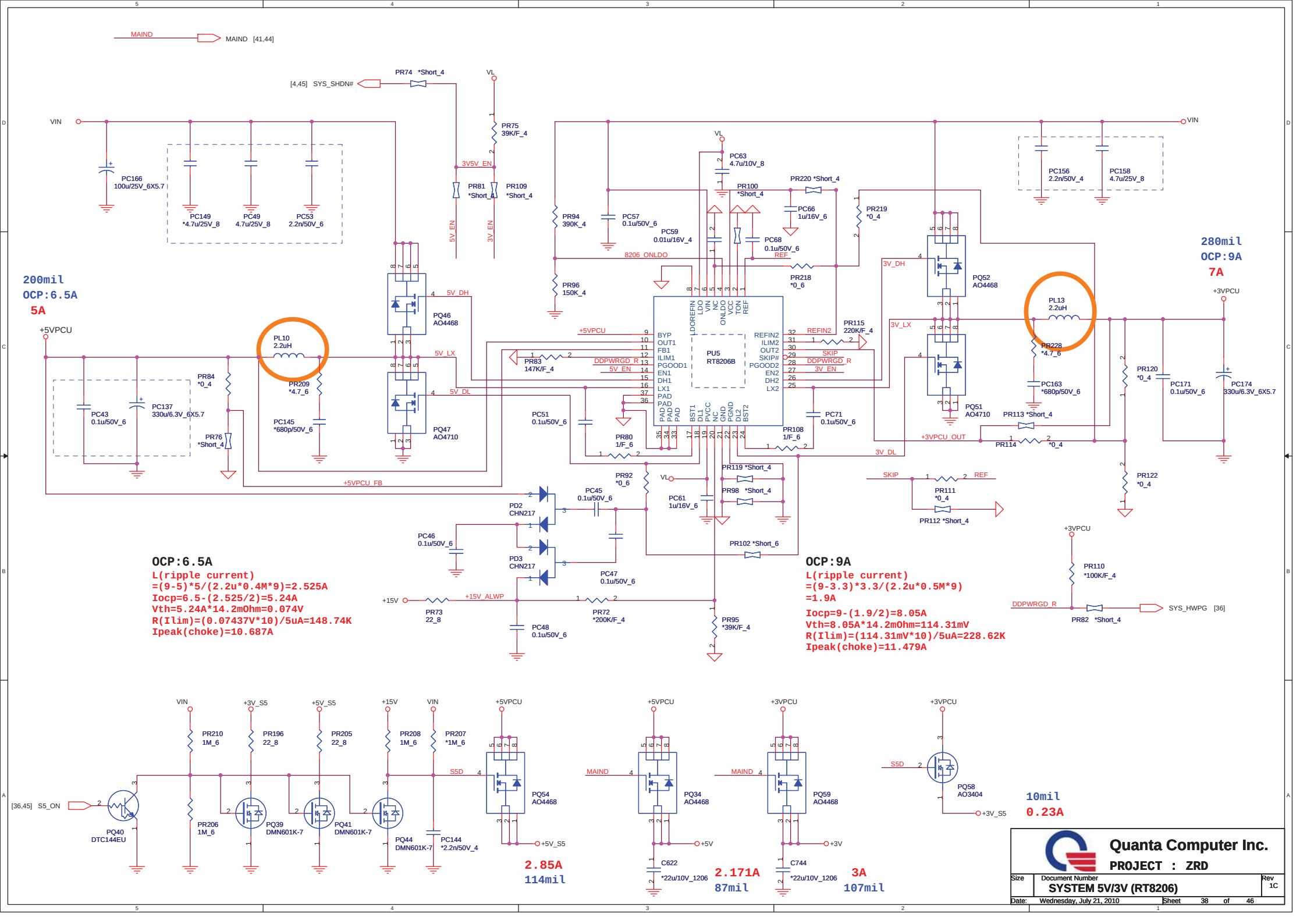

## INTERNAL KEYBOARD STRIP SET(KBC)

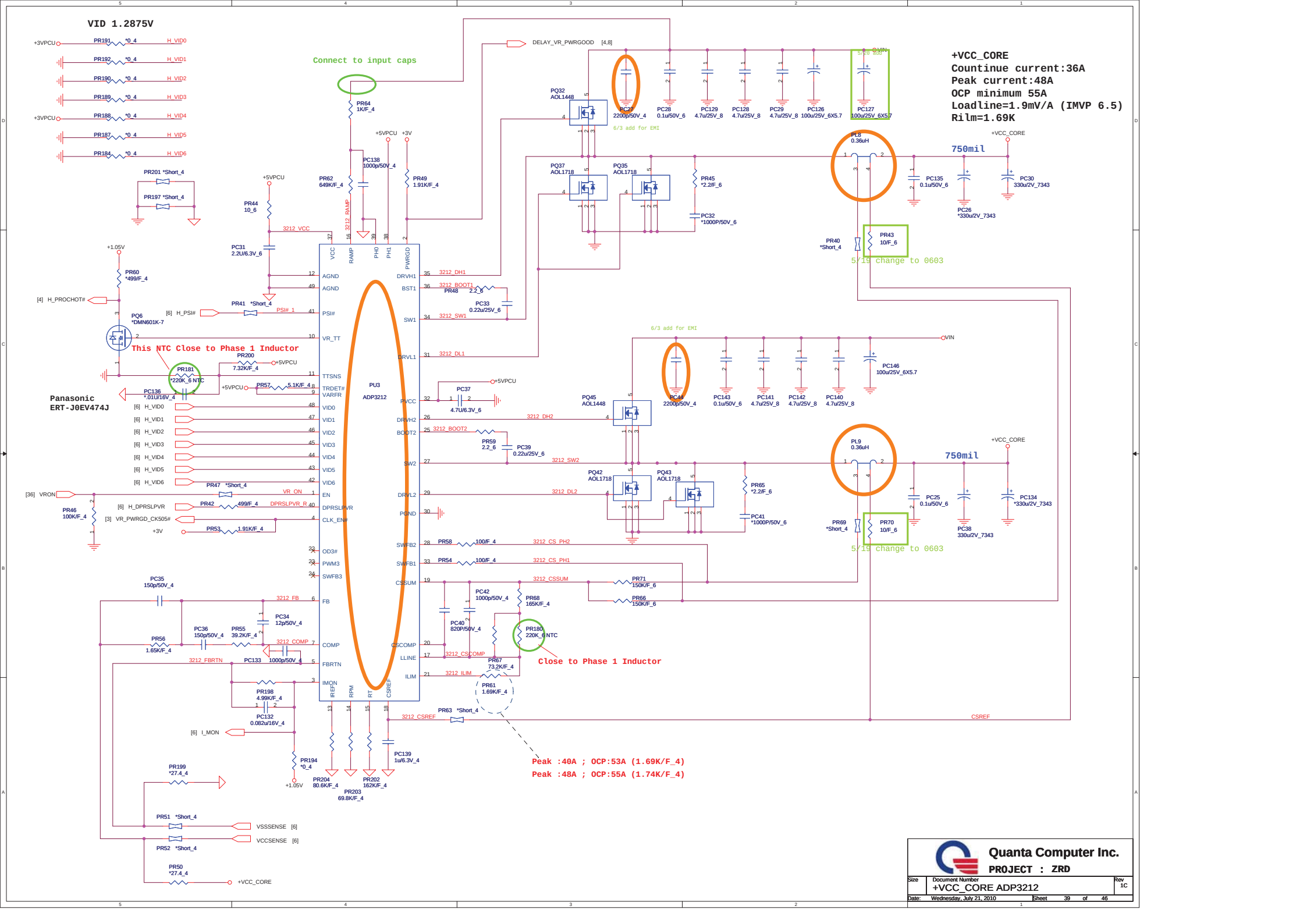
Quanta Computer Inc.
PROJECT : ZRD

| Size | Document Number | Rev |
|---|---|---|
| | WPCE781 & FLASH | 1C |

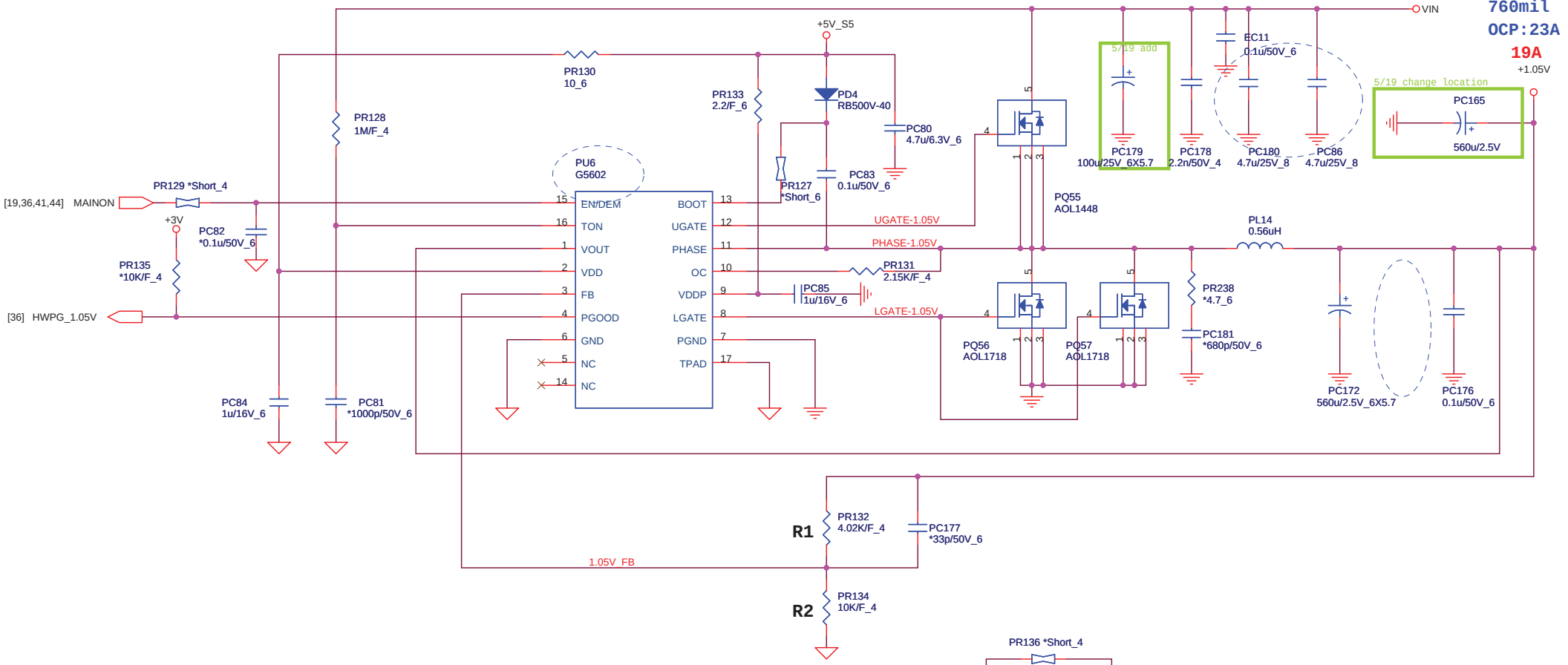
Date: Wednesday, July 21, 2010 Sheet 36 of 46


SP@POWER_JACK
dcjk-2dc2003-000111-3p-v
PJ1
PL2
HI0805R800R-00_8
PL1
HI0805R800R-00_8
VA1
PD5
SBR1045SP5-13
PD6
SMAJ20A
PD1
SW1010CPT
PC88
0.1u/50V_6
PC89
2200p/50V_6
PC90
47u/25V_6.3*6
5/12 EMI RESERVE
PC91
0.1u/50V_6
VA2
200mil
PC1
0.1u/50V_6
PR3
220K_4
PR2
220K_4
PQ17
FDD6685
0.01_3720
PR151
PR152
SHORT_PAD_4
PR150
SHORT_PAD_4
5/14 add short PAD
CSIN_1
CSIP_1
PR1
*Short_4
D/C# [36]
PQ1
IMD2AT108
VIN
300mil
PC99
0.1u/50V_6
PC98
2200p/50V_6
PR155
33K/F_4
PQ20
FDD6685
PR154
10K_4
PQ21
DMN601K-7
PR5
10/F_4
PR6
10/F_4
PC7
0.1u/50V_6
PC4
1u/16V_6
PR14
4.7_6
PC9
1u/16V_6
ISL88731_VDDP
PD7
*RB500V-40
PC3
0.1u/50V_8
PC95
2200p/50V_6
PC96
*0.1u/50V_6
PC8
4.7u/25V_8
+3VPCU
PC15
0.1u/50V_6
PR7
2.7_6
88731B_2
88731B_1
PR22
100K_4
[36] ACIN
MBDATA
MBCLK
PR4
49.9/F_6
DCIN
PC2
0.1u/50V_6
PR13
82.5K/F_4
88731ACSET
PR15
22K/F_4
PU2
ISL88731A
VDDSMB
SDA
SCL
ACOK
DCIN
ACIN
VREF
ICOMP
NC
VCOMP
BOOT
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC
VBF
GND
ISL88731_UGATE
ISL88731_PHASE
ISL88731_LGATE
PQ18
AO4468
PQ19
AO4468
PL3
6.8uH
0.01_3720
PR156
140mil
BAT-V
PR153
*4.7_6
PC93
*680p/50V_6
PR19
10/F_4
PR20
10/F_4
PR158 *Short_4
PR157
100_4
PC11
0.1u/50V_6
CSOP_1
BAT-V
PC97
2200p/50V_6
PC101
10u/25V_1206
PC100
10u/25V_1206
PC92
0.1u/50V_6
PC94
100p/50V_6
PL4
HI0805R800R-00_8
PL5
HI0805R800R-00_8
MBAT+
C114F3-108A1-L_Batt_Conn
PJ2
PR9
100_4
TEMP_MBAT
TEMP_MBAT [36]
PR12
100K_4
+3VPCU
PC5
47p/50V_6
PC6
47p/50V_6
PR8
*Short_4
PR11
100_4
PR10
100_4
MBCLK [36]
MBDATA [36]
PC21
2.21K/F_4
PC14
0.01u/50V_6
PC10
*1u/16V_6
PC12
0.01u/50V_6
PC13
*0.01u/50V_6
ICMNT
ICMNT [36]
ISL88731 thermal pad
tie to Pin12
PU1
CM1293A-04SO
CH1
CH2
CH3
CH4
VN
VP
MBDATA
+3VPCU
MBCLK
TEMP_MBAT
Add ESD diode base on EC FAE suggestion
Quanta Computer Inc.
PROJECT : ZRD
Size
Document Number
Charger(ISL88731A)
Rev
1C
Date: Wednesday, July 21, 2010
Sheet 37 of 46


MAIND
MAIND [41,44]
[4,45] SYS_SHDN#
PR74 *Short_4
VL
VIN
PR75 39K/F_4
3V5V_EN
PR81 *Short_4
PR109 *Short_4
5V_EN
3V_EN
PC166 100u/25V_6X5.7
PC149 *4.7u/25V_8
PC49 4.7u/25V_8
PC53 2.2n/50V_6
200mil
OCP:6.5A
5A
+5VPCU
PL10 2.2uH
PR84 *0_4
PR209 *4.7_6
PC43 0.1u/50V_6
PC137 330u/6.3V_6X5.7
PC145 *680p/50V_6
PR76 *Short_4
PQ46 AO4468
PQ47 AO4710
5V_DH
5V_LX
5V_DL
+5VPCU_FB
PR94 390K_4
PR96 150K_4
PC57 0.1u/50V_6
PC59 0.01u/16V_4
8206_ONLDO
PC63 4.7u/10V_8
PR100 *Short_4
PR220 *Short_4
PC66 1u/16V_6
PC68 0.1u/50V_6
REF
PR218 *0_6
PR219 *0_4
PU5 RT8206B
LDOREFIN LDO VIN NC ONLDO VCC TON REF
BYP OUT1 FB1 ILIM1 PGOOD1 EN1 DH1 LX1 PAD PAD PAD PAD
REFIN2 ILIM2 OUT2 SKIP# PGOOD2 EN2 DH2 LX2
BST1 DL1 PVCC NC GND PGND DL2 BST2
PR83 147K/F_4
DDPWRGD_R
PR80 1/F_6
PC51 0.1u/50V_6
PC71 0.1u/50V_6
PR108 1/F_6
REFIN2
PR115 220K/F_4
SKIP
3V_EN
3V_DH
3V_LX
3V_DL
PQ52 AO4468
PQ51 AO4710
PR113 *Short_4
PR114 *0_4
+3VPCU_OUT
280mil
OCP:9A
7A
PL13 2.2uH
PR228 *4.7_6
PC163 *680p/50V_6
PR120 *0_4
PC171 0.1u/50V_6
PC174 330u/6.3V_6X5.7
PR122 *0_4
PC156 2.2n/50V_4
PC158 4.7u/25V_8
PR92 *0_6
PC61 1u/16V_6
PR119 *Short_4
PR98 *Short_4
PR102 *Short_6
PC45 0.1u/50V_6
PC46 0.1u/50V_6
PC47 0.1u/50V_6
PD2 CHN217
PD3 CHN217
+15V
+15V_ALWP
PR73 22_8
PR72 *200K/F_4
PC48 0.1u/50V_6
PR95 *39K/F_4
SKIP
REF
PR111 *0_4
PR112 *Short_4
PR110 *100K/F_4
DDPWRGD_R
PR82 *Short_4
SYS_HWPG [36]
OCP:6.5A
L(ripple current)
=(9-5)*5/(2.2u*0.4M*9)=2.525A
Iocp=6.5-(2.525/2)=5.24A
Vth=5.24A*14.2mOhm=0.074V
R(Ilim)=(0.07437V*10)/5uA=148.74K
Ipeak(choke)=10.687A
OCP:9A
L(ripple current)
=(9-3.3)*3.3/(2.2u*0.5M*9)
=1.9A
Iocp=9-(1.9/2)=8.05A
Vth=8.05A*14.2mOhm=114.31mV
R(Ilim)=(114.31mV*10)/5uA=228.62K
Ipeak(choke)=11.479A
[36,45] S5_ON
PQ40 DTC144EU
PR210 1M_6
PR206 1M_6
PQ39 DMN601K-7
PR196 22_8
PR205 22_8
PQ41 DMN601K-7
PR208 1M_6
PQ44 DMN601K-7
PR207 *1M_6
PC144 *2.2n/50V_4
S5D
PQ54 AO4468
+5V_S5
2.85A
114mil
PQ34 AO4468
C622 *22u/10V_1206
+5V
2.171A
87mil
PQ59 AO4468
C744 *22u/10V_1206
+3V
3A
107mil
PQ58 AO3404
+3V_S5
10mil
0.23A
Quanta Computer Inc.
PROJECT : ZRD
Size
Document Number
SYSTEM 5V/3V (RT8206)
Rev 1C
Date: Wednesday, July 21, 2010
Sheet 38 of 46


VID 1.2875V
Connect to input caps
+VCC_CORE
Countinue current:36A
Peak current:48A
OCP minimum 55A
Loadline=1.9mV/A (IMVP 6.5)
Rilm=1.69K
This NTC Close to Phase 1 Inductor
Panasonic
ERT-J0EV474J
Close to Phase 1 Inductor
Peak :40A ; OCP:53A (1.69K/F_4)
Peak :48A ; OCP:55A (1.74K/F_4)
5/19 change to 0603
6/3 add for EMI
750mil
PU3
ADP3212
Quanta Computer Inc.
PROJECT : ZRD
+VCC_CORE ADP3212
Wednesday, July 21, 2010

# [PWM]




TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

TON=3.85p*1M*1/(Vin-0.5)

Frequency=1/(0.0036767)=272K

AO1718 Rdson=3~4.3mOhm

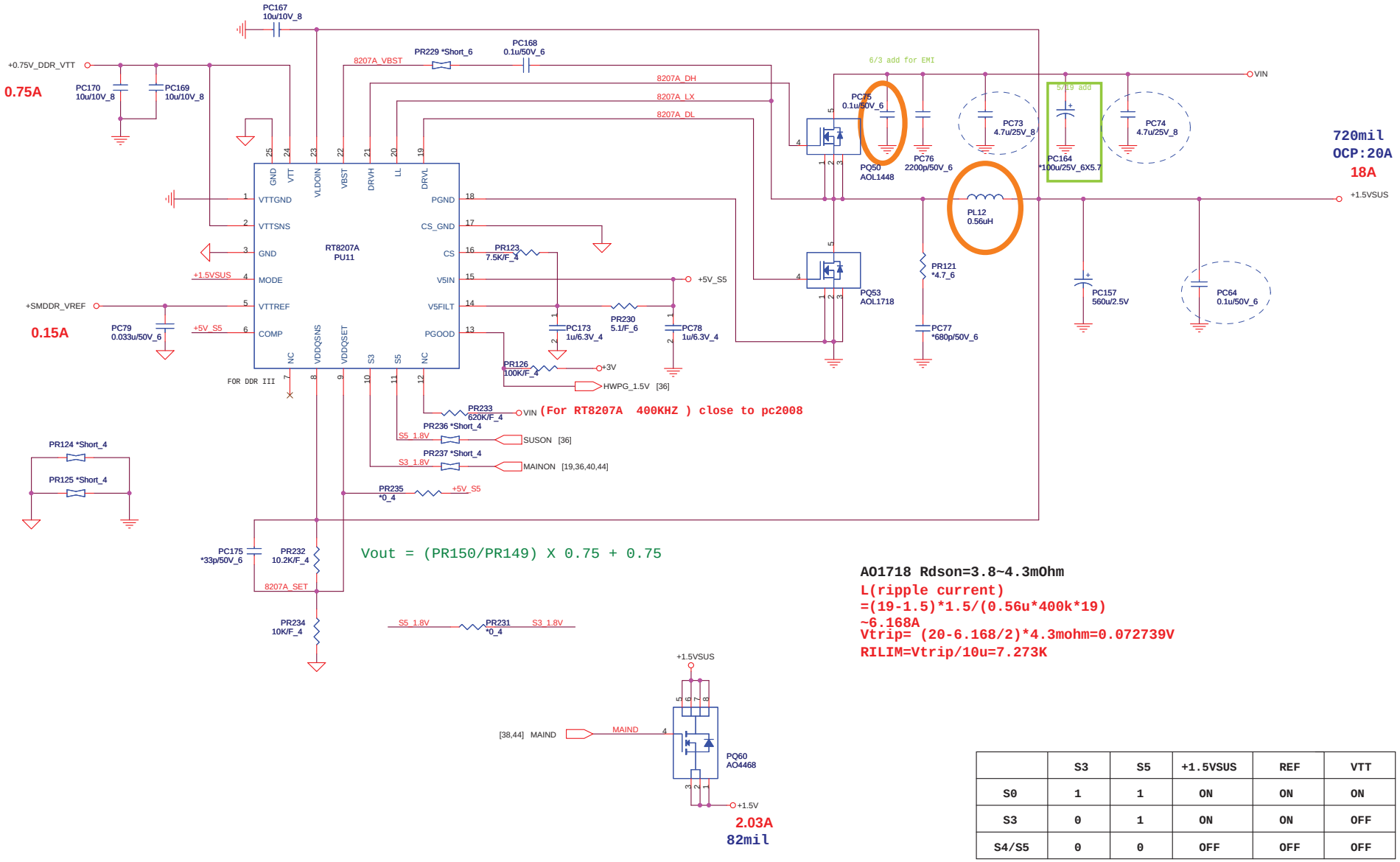
L(ripple current)
=(19-1.05)*1.05/(0.56u*272k*19)
~6.512A

RILIM=2.15mohm*23-3.256/20uA=2.122Kohm

I(choke)peak=29.512A

| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT : ZRD | | |
| Size | Document Number: +VTT (UP6111A) | Rev: 1C |
| Date: Wednesday, July 21, 2010 | Sheet 40 of 46 | |

[PWM]




AO1718 Rdson=3.8~4.3mOhm

L(ripple current)
=(19-1.5)*1.5/(0.56u*400k*19)
~6.168A
Vtrip= (20-6.168/2)*4.3mohm=0.072739V
RILIM=Vtrip/10u=7.273K

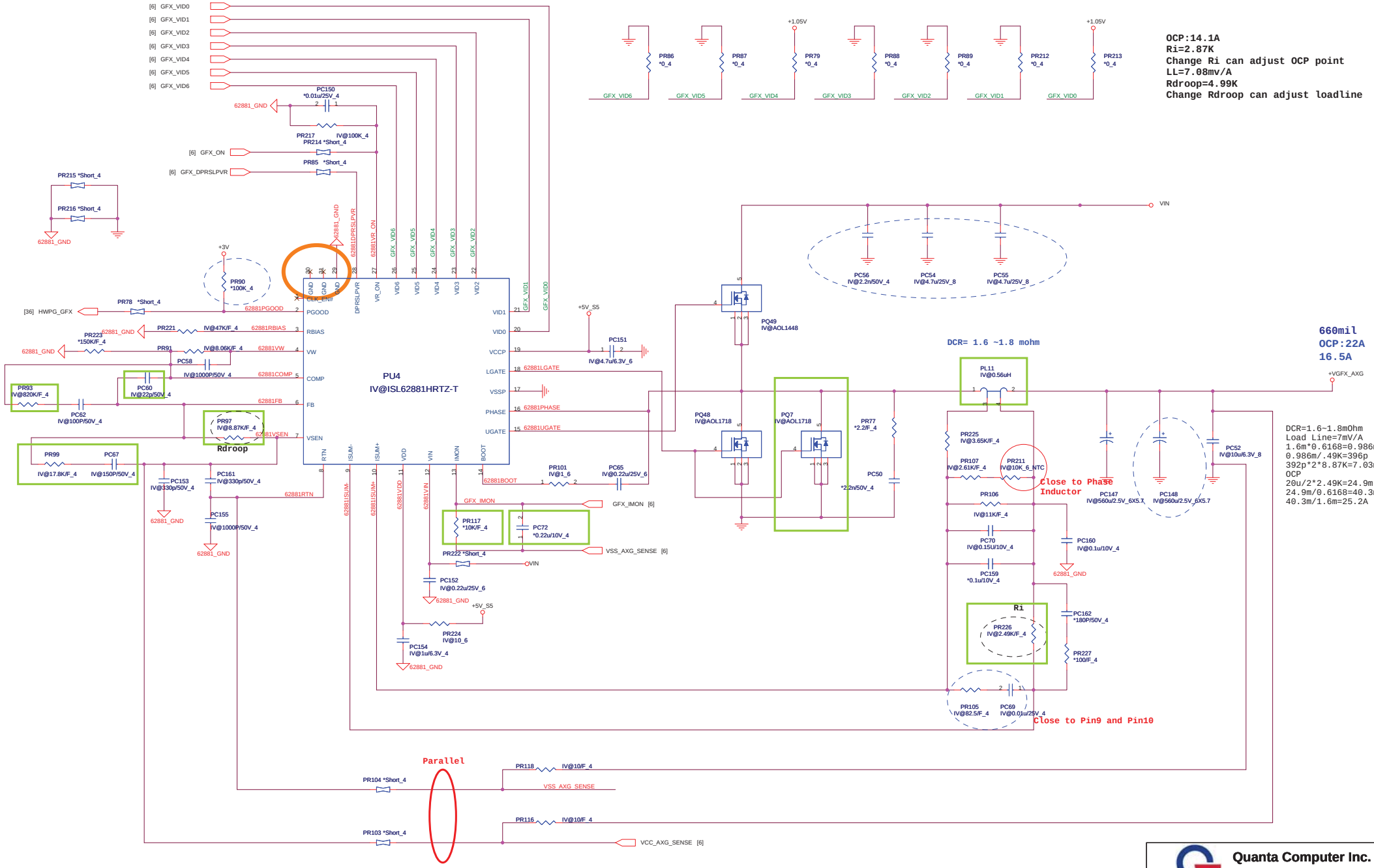
| | S3 | S5 | +1.5VSUS | REF | VTT |
|---|---|---|---|---|---|
| S0 | 1 | 1 | ON | ON | ON |
| S3 | 0 | 1 | ON | ON | OFF |
| S4/S5 | 0 | 0 | OFF | OFF | OFF |

Quanta Computer Inc.
PROJECT : ZRD

| Size | Document Number | Rev |
|---|---|---|
| | DDR 1.5V(RT8207A) | 1C |

Date: Wednesday, July 21, 2010 Sheet 41 of 46

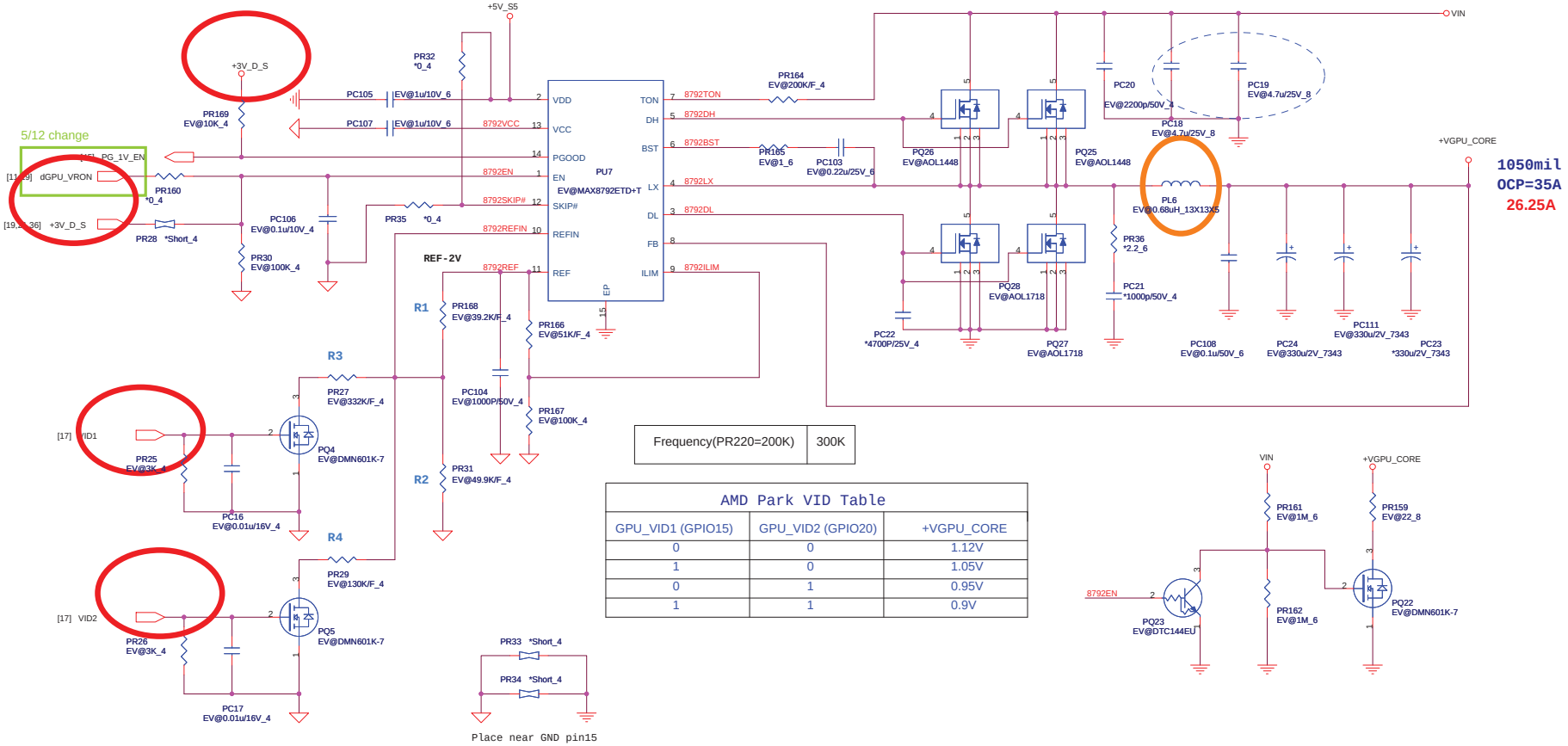
# Int_VGA [PWM]




Quanta Computer Inc.
PROJECT : ZRD

| Size | Document Number | Rev |
|---|---|---|
| | +VGFX_AXG (ISL62881) | 1C |
| Date: Wednesday, July 21, 2010 | Sheet 42 of 9 | |

1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.




| Frequency(PR220=200K) | 300K |
|---|---|

AMD Park VID Table

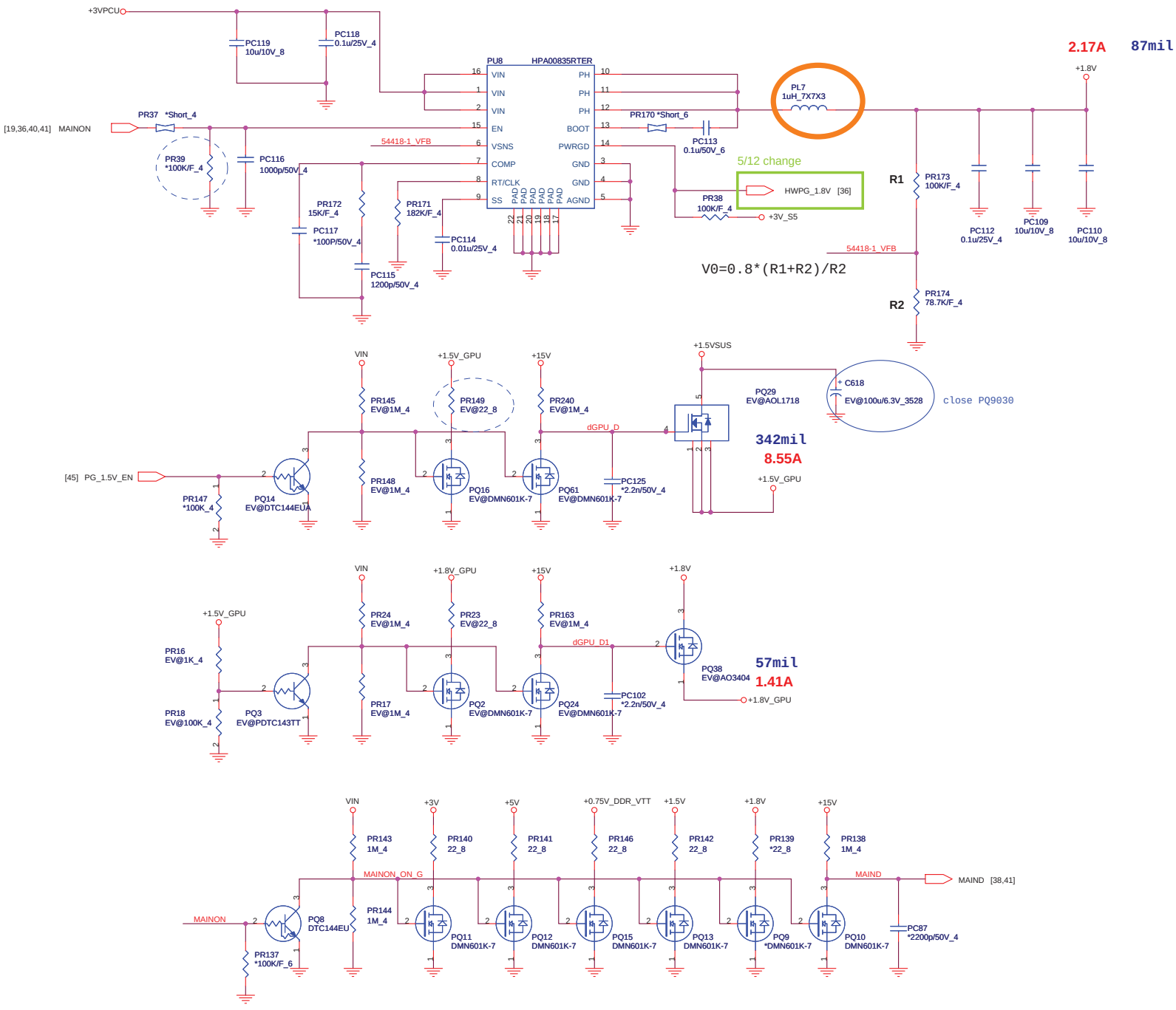
| GPU_VID1 (GPIO15) | GPU_VID2 (GPIO20) | +VGPU_CORE |
|---|---|---|
| 0 | 0 | 1.12V |
| 1 | 0 | 1.05V |
| 0 | 1 | 0.95V |
| 1 | 1 | 0.9V |

Quanta Computer Inc.

PROJECT : ZRD

| Size | Document Number | Rev |
|---|---|---|
| | GPU CORE(MAX8792) | 1C |

Date: Wednesday, July 21, 2010 Sheet 43 of 9




7/7 modify

**Quanta Computer Inc.**

**PROJECT : ZRD**

| Size | Document Number | Rev |
|---|---|---|
| | Discharge/1.8V) | 1C |

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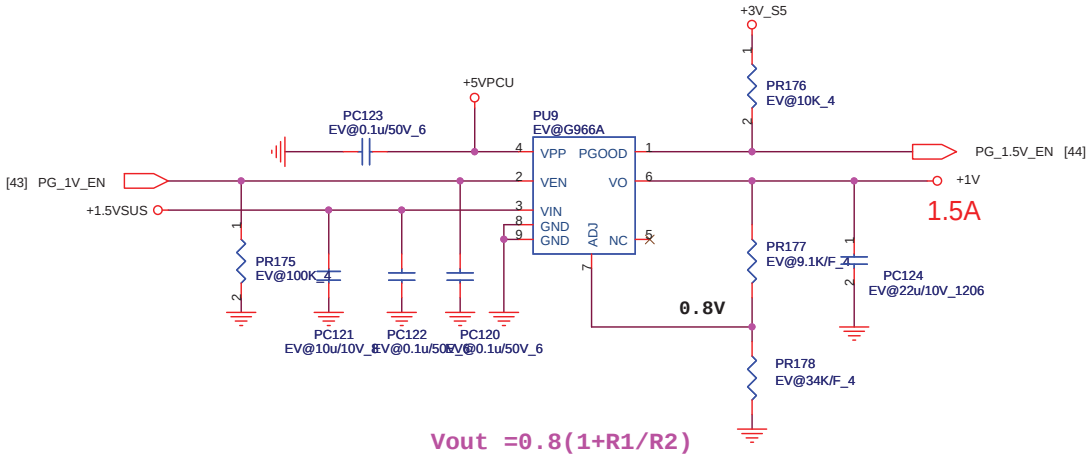
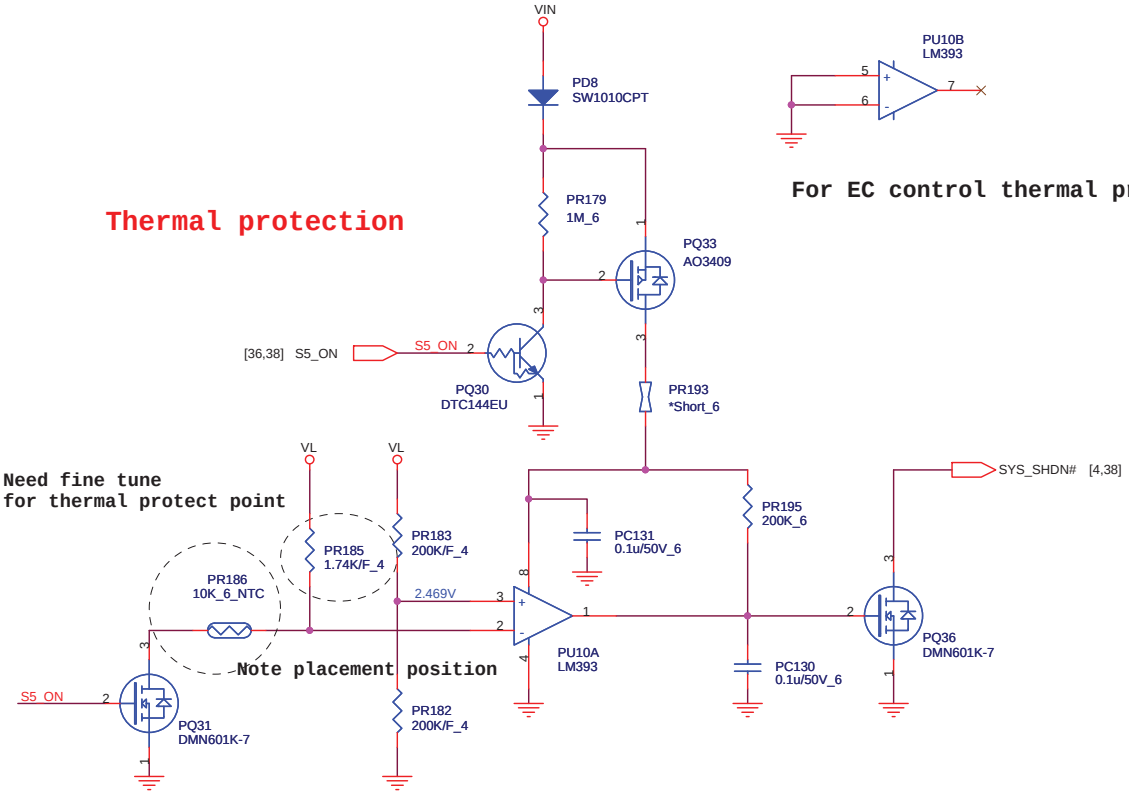



Vout =0.8(1+R1/R2)
=1V




Quanta Computer Inc.

PROJECT : ZRD

| Size | Document Number | Rev |
|---|---|---|
| | | 1C |

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| Model | REV | CHANGE LIST |
|---|---|---|
| ZRD MB | 1A | FIRST RELEASED |
| | 2A | Page 3 : Unstuff L54 & stuff R586 & change U31 P/N for 3V_CLK gen and Switch CLK_BUF_DREFSSCLK and CLK_BUF_PCIE_3GPLL<br>Page 4 : Q16 Change P/N for EOD part & short R116 (Del.) for 0 ohm<br>Page 9 : Short R244 (Del.) for 0 ohm<br>Page 10 :Short R243 (Del.) for 0 ohm<br>Page 12 :Short R189 ,R190 & R534 (Del.) for 0 ohm & C655 change P/N for EOD part<br>Page 14 :Del. R268 & R247 for M3 solution & stuff R269 ,R229 ,R223 & R226 for M1 solution,Stuff C372 for +1.5VSUS leakage<br>Page 15 :Stuff C459 for +1.5VSUS leakage<br>Page 25 :Q12 ,Q17 & Q18 Change P/N for ESD , CN10 Change P/N ,Q14.2 & Q13.2 Change from +5V to +3V<br>Page 27 :C339 & C381 of footPrint Change from 0805 to 0402 for ESD<br>Page 28 :Unstuff R566 ,R294 ,R284 ,R278 ,R276 ,R273 ,R272 for disable debug card function<br>Page 29 :C303 & C254 Change P/N for EOD , CN11 Change footprint for ME design request.<br>Page 30 :U13 Change AMP circuit<br>Page 31 :Q22 & Q23 Change P/N for EOD part.<br>Page 34 :Del. LS5 , CN12 Change P/N<br>Page 36 :C27 Change P/N for EOD part<br>Page All : Change to short pad : Location : R458 ,R452 ,R537 ,R533 ,R144 ,R155 ,R191 ,R140 ,R201 ,R224 ,R461 ,R136 ,R197 ,R206 ,R219 ,R212 ,R166 ,R174 ,R188 ,R202 ,R209 ,R184 ,R168 ,R185 ,R448 ,R447 ,R5 ,R10 ,R9 ,R6 ,R263 ,R288 ,R544 ,R436 ,R563 ,R570 ,R569 ,R584 ,R299 ,C738 ,R311 ,R585 ,R583 ,R571 ,R582 ,R575 ,R576 ,R579 ,R333 ,R352 ,R331 ,R332 & R349 |
| | 3A | |
| | 3C | |

| MODEL | ZRD FROM | ZRD To |
|---|---|---|
| | X | 1A |
| | X | 1A |
| | 1A | 2A |
| | 1A | 2A |
| | 1A | 2A |
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| | 1A | 2A |
| | 1A | 2A |
| | 1A | 2A |
| | 1A | 2A |
| | 2A | 3A |
| | 2A | 3A |
| | 2A | 3